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Claims 19-25

Problem: See Page lines 7-25

" 2 " 1-24

" 3 " 1-21

Solution: " " 6 " 9-19

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Searcher: Derrick Blalock

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Attorney Docket No.: AVX-122

TITLE: VIA COMPONENTS FOR INTEGRATED PASSIVE COMPONENTS

BACKGROUND OF THE INVENTION

The present invention relates to electrical connections made on printed circuit boards (PCBs) or within integrated passive devices (IPDs) for the purposes of connecting various electrical components. Specifically, the present invention relates to the use of vias to connect electronic components on and within multi-layer electrical devices, including IPDs. More specifically, the present invention relates to the use of blind vias to house electronic components in an effort to provide vertical electrical connections within electronic devices.

With the ever-increasing demand for additional features and the expectations of longer battery life in present day electronic devices, circuit and component designers have responded with smaller component designs requiring less voltage. The result has been not only an increase in device operation speed or operating frequency, but also an increase in package density. In addition to integrated circuitry, the use of multi-layered printed circuits has aided in reducing the space requirements of advanced circuitry for portable electronic devices.

In today's typical multi-layer printed circuit boards, the components, both active and passive, are soldered to the surface of the circuit board. Conductive paths are formed on the surface, usually by photolithography, and are connected by conductive vias to internal conductors, which form a complex series of three-dimensional interconnections.

As a result of the reduction in relative sizes, however, a point has been reached where the components themselves are difficult to handle and the lands to which they must be attached have not been capable of a comparable reduction in size. Further, the available line and space widths of the conductive paths have reached a practical limit of about 5-10 mils, without going to special, and expensive high density processing.

In an attempt to resolve these problems, two main approaches have been undertaken: first, designers have begun using integrated passive devices (IPDs) in which multiple passive components are incorporated into a single package for positioning within the circuit. Second, designers have incorporated special layers within the circuit board itself to provide capacitive and resistive functions, which may be customized as required. These approaches serve only to save space on the surface of the PCB itself.

Unfortunately, neither of these two approaches solves both the need for space savings and increased flexibility in introducing components other than capacitors and resistors into the PCB or IPD. For example, the use of an IPD on a PCB is not attractive where its design would require significant re-routing of the surface traces thus off-setting the intended space savings. Additionally, it is inevitable that when multiple components are placed within the same package there will be parasitics that occur. These are detrimental to the performance of the device.

Further, integrated passive devices are currently limited to providing only capacitive and resistive functions. Such a limitation fails to address the need to save space regardless of the component's function. Finally, there are economic

limitations to the use of IPDs. For instance, as a custom product, integrated passive devices are a long-delivery item which increase both cost and manufacturing time of a product. Still further, in the electronics industry, customers of component manufacturers are loath to spend more money on an unproven multi-component device as opposed to individual components with proven reliability, and tight parametric tolerances.

Similarly, the use of buried layers within the circuit board itself has numerous drawbacks. The range of available capacitive and resistive values available in the buried layers is limited and they must be preset. Additionally, the sculpting of these layers is a very cost and time-intensive process which is currently beyond the capabilities of most PCB manufacturers. For example, the board manufacturers are used to dealing with board layers of at least 250 microns while the thickness of a buried capacitive layer would need to be on the order of 50 microns or smaller to be effective. Additionally, because of their being so thin, such a layer is very fragile. Any breakage would result in an electrical fault and would require the board to be scrapped.

During further finishing of the PCB, such layers may be subjected to intense heat or other treatments required for completing the manufacturing process. Because of this treatment, the capacitive and resistive values of the layers may be inadvertently altered from the desired preset values of the layers. The PCB would then be unable to effectively operate as designed.

SUMMARY OF THE INVENTION

The present invention recognizes and addresses various of the foregoing

limitations and drawbacks, and others, concerning a method of using a via to house an electronic component. Therefore, the present invention provides a method for using a blind via for housing and allowing electrical connection of a passive electronic component within a layer of either a printed circuit board or an integrated passive device.

It is, therefor, one aspect of the subject invention to provide a method for reducing the space demands on the surface of a PCB. More particularly, it is an aspect of the present invention to provide a method of using a via to house an electronic component within a layer of a printed circuit board thus reducing the space demands on the surface of the PCB.

It is yet another aspect of the present invention to provide a method of housing an electronic component in a via such that vertical electrical connection is made between adjacent components and/or buried conductors. In such context, it is a further aspect of the present invention to provide a method of producing a vertical electrical connection between a passive electronic component and both an active component and a buried conductor.

It is still another aspect of the present invention to provide a method of using a via to house an electronic component in which such method allows for greater flexibility in using integrated passive devices on printed circuit boards. In such context, it is a further aspect of the present invention to provide such a method in which resistors, capacitors, varistors, thermistors or other passive components may be housed within such a via within a layer of the PCB itself.

An additional aspect of the present invention includes providing a method for housing an electronic component in a blind via so as to reduce production costs

of typical PCBs. In such context, it is a further aspect of the present invention to provide such a method that additionally provides greater yields (i.e., ranges of component values), greater flexibility in design due to space-savings and the opportunity to utilize a greater variety of components within the design.

It is still a further aspect of the present invention to provide a method for increasing the flexibility of integrated passive devices. More particularly, it is an aspect of the present invention to provide a method of using vias to house electronic components between layers within an integrated passive device.

It is yet another aspect of the present invention to provide a method of using a via to house an electronic component in which such method allows for greater flexibility in the design and manufacture of integrated passive devices.

Additional aspects and advantages of the invention are set forth in, or will be apparent to those of ordinary skill in the art from the detailed description that follows. Also, it should be further appreciated that modifications and variations to the specifically illustrated and discussed steps, features and materials hereof may be practiced in various embodiments and uses of this invention without departing from the spirit and scope thereof, by virtue of present reference thereto. Such variations may include, but are not limited to, substitutions of equivalent steps, means, features, and materials for those shown or discussed, and the functional or positional reversal of various parts, features, or the like.

Still further, it is to be understood that different embodiments, as well as different presently preferred embodiments, of this invention, may include various combinations or configurations of presently disclosed steps, features, elements, or their equivalents (including combinations of steps, features or configurations

thereof not expressly shown in the figures or stated in the detailed description).

These and other features, aspects and advantages of the present invention will become better understood with reference to the following description and appended claims. The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, serve to explain the principles of the invention.

The present invention is directed toward a method for using a via to house an electronic component, generally a passive component, within a layer of an electrical device in such a manner as to allow vertical electrical connection between the component and other elements of the device. In particular, one embodiment of the present invention provides for the use of blind vias to house passive components, which may be electrically connected to both an embedded ground plane located within the PCB and active components located on an outer surface of the PCB.

Another embodiment of the present invention is directed toward a method for using vias to house electronic components, which may be electrically connected to other passive components within an integrated passive device in such a manner as to allow vertical electrical connection between the component and other of the elements within the device.

BRIEF DESCRIPTION OF THE DRAWINGS

A full and enabling disclosure of the present invention, including the best mode thereof, directed to one of ordinary skill in the art, is set forth in the specification, which makes reference to the appended figures, in which:

FIG. 1 is an overhead view of a portion of a typical printed circuit board using horizontal electrical connections between an active and multiple passive components;

FIG. 2 is a cross-section view taken along line A-A of the printed circuit board as shown in Figure 1;

FIG. 3 is an overhead view of a portion of a printed circuit board with electrical connection between an active and multiple passive components in accordance with the present invention;

FIG. 4 is a cross-section view taken along line B-B of the printed circuit board as shown in Figure 3;

FIG. 5 is an exemplary enlarged cross-section view of an electronic component placed in a via in accordance with the present invention;

FIG. 6 is an overhead view of an exemplary layer of an integrated passive device in accordance with the present invention providing a portion of the device's circuitry and capture pads for electrical connection to other components of the device;

FIG. 7 is an overhead view of an exemplary layer of an integrated passive device in accordance with the present invention that has vias drilled therethrough;

FIG. 8 is an overhead view of a bonded combination of the layers from Figures 6 and 7 showing the corresponding vias and capture pads and generally representing an exemplary skeletal structure of an integrated passive device made in accordance with the present invention;

FIG. 9 is an overhead view of the IPD of Figure 8 with additional

exemplary resistor/conductor patterns placed on an outer surface of the IPD and band terminated edges;

FIG. 10 is a side view of the IPD of Figure 9 showing the introduction of the vertically oriented passive components into their respective via for electrical connection to the capture pads on the IPD layer of Figure 6;

FIG. 11 is an overhead view of the IPD of Figure 8 including the passive components in their respective via;

FIG. 12 is an overhead view of the IPD of Figure 11 showing the top contacts connecting the via-located passive components with their respective terminations or resistive/conductive elements; and

FIG. 13 is an exemplary enlarged cross-sectional view of one of the via-located electronic components of Figure 12 in accordance with the present invention.

Repeat use of reference characters throughout the present specification and appended drawings is intended to represent the same or analogous features or elements of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to presently preferred embodiments of the invention, examples of which are fully represented in the accompanying drawings. Such examples are provided by way of an explanation of the invention, not limitation thereof. In fact, it will be apparent to those skilled in the art that various modifications and variations can be made in the present invention, without departing from the spirit and scope thereof. For instance, features illustrated or

described as part of one embodiment can be used on another embodiment to yield a still further embodiment. Still further, variations in selection of materials and/or characteristics may be practiced, to satisfy particular desired user criteria. Thus, it is intended that the present invention cover such modifications and variations as come within the scope of the present features and their equivalents.

As disclosed above, the present invention is particularly concerned with a method for housing an electronic component within a via in order to reduce the space demands placed on either the surface of a printed circuit board or to enhance the flexibility of electrical connections between components within an integrated passive device.

An overhead planar view of a typical printed circuit board 10 (PCB) using known design concepts is shown in Figure 1. Generally, such PCBs serve as substrates to support integrated circuits comprising both active 12 and passive 14 components that are electrically connected by leads 16 to lands 18 on a surface 20 of the PCB 10. Such electrical connections are made most often by soldering the integrated circuit component's leads 16 to the lands 18 on a surface 20 of the PCB 10.

Figure 2 shows a cross-sectional view of the PCB in Figure 1, in which the PCB 10 comprises multiple non-conductive laminae 22, 24 and 26 between which various patterned conductive layers 28, 30 and 32 exist. One of ordinary skill in the art would recognize this multi-layer PCB 10 as typical of the current PCBs in use throughout the electronics industry. The materials and patterns used to construct such laminae 22, 24 and 26 and embedded conductive layers 28, 30 and 32 are well known to one of ordinary skill in the art and form no particular aspect of the

present invention. However, it should be noted that any of the known materials and methods of forming either the laminae 22, 24 and 26 or the embedded patterned conductive layers 28, 30 and 32 may be used in the present invention.

For illustrative purposes only, presume embedded conductive layers 28 and 32 are for carrying signals from one portion of the circuitry to another. Similarly presume, however, that conductive layer 30 is a ground plane. In the present constructs, there typically may exist between each land 18 and the ground plane 30 at least one passive component 14.

As can be seen in Figure 1, which has been greatly simplified for explanatory purposes only, there exist eight passive components 14, one between each land 18 and the ground plane 30. Each passive component 14 is additionally connected to a ground, shown here as trace 34. Trace 34 exists on an upper surface 20 of the printed circuit board 10. The ground trace 34 is connected to the embedded ground plane 30 by way of a hole or via 36 through both the ground trace 34 and at least one of the non-conductive layers 24 of the PCB 10.

Using present design techniques, it is in this manner that both active 12 and passive 14 components are generally connected to a buried ground plane 30 in order to aid in the elimination of random noise, interference or extraneous voltages from the circuit. As can be seen, however, such a design layout places greater physical space demands on the upper surface 20 of the PCB 10 itself. Additionally, as the circuit designs become more and more complex the need for additional space dedicated to connectivity areas (i.e., lands) can only increase.

Secondary structures are also represented in Figure 1. Additional traces 38 may also be connected to the ground plane 30 by way of a hole or via 40. In some

cases a via 42 may pass through all of the laminea 22, 24 and 26 and the patterned conductive layers 28, 30 and 32 to connect circuitry on opposing faces of the PCB. In such an instance, as shown here, there may be an opening 44 through the ground plane 30 to prevent any contact by the electrically conductive connecting means 46 therein with the ground plane 30 itself as such contact would result in a short circuit.

In one exemplary embodiment of the present invention, as shown in Figures 3 and 4, a printed circuit board 10 is acting to support an integrated circuit constructed in accordance with the present invention. As before, the integrated circuit may be comprised of a plurality of active 12 and passive 14 components connected electrically by soldering the component leads 16 to lands 18 on a surface 20 of the PCB 10. Figure 4 shows a cross-sectional view of the PCB 10 in Figure 3 constructed in accordance with the present invention, in which the printed circuit board 10 comprises multiple non-conductive laminae 22, 24 and 26 between which various patterned conductive layers 28, 30 and 32 exist.

Unlike the typical PCB construction as shown in Figures 1 and 2, the present PCB 10 and integrated circuit instead houses the passive components 14 in a blind via 48 within non-conductive layer 22 of the PCB 10. In this preferred exemplary embodiment of the present invention, the use of such vias 48 is limited to non-conductive layer 22. It should be noted, however, that the present invention does not limit integration of passive components 14 within the printed circuit board 10 to only the upper non-conductive layer 22. Further, such integration of components reduces demand for space on the surface 20 of the PCB 10.

As a result of this integration into the PCB, the passive components 14 are mounted in a vertical orientation in relation to the surface 20 of the PCB 10. It would be obvious to one of ordinary skill in the art that the surface trace 34 is no longer required to connect each passive component 14 to the via 36 and on to the embedded ground plane 30. Instead, by virtue of their vertical orientation, the passive components 14 are now directly adjacent the ground plane 30 and may be electrically connected thereto.

In order to accommodate the passive components 14 into the non-conductive layer 22, preparation of the blind via 48 must take place during the manufacturing of the PCB 10 itself. Generally, all of the unique features of each non-conductive layer 22, 24 and 26 of the PCB 10 are formed prior to their being brought together to form the PCB 10. Each via is drilled into and each of the patterned conductive layers 28, 30 and 32 is formed on the upper surface of its respective non-conductive layer 22, 24 and 26 prior to their being stacked to form the PCB 10.

The passive elements 14 may be placed into a via 48 in their vertical orientation and soldered to the underlying ground plane 30 using a high temperature solder or connection may be made by virtue of a conductive epoxy material 62. This will aid in preventing any undesired effects subsequent soldering may have to these connections when connecting the "upper" termination of the passive components 14 to the lands 18.

The exemplary non-conductive layer 22 into which the blind via 48 are drilled is typically a rigid epoxy pre-impregnated material, such as FR4, an epoxy-

fiberglass composite. The choice of such material is in part designed to ensure that the vias 48 drilled before the various laminea 22, 24 and 26 are stacked, do not collapse before the introduction of the passive components 14 therein. In the present invention, closure of such vias upon exposure to the increased heat from the PCB formation process or from the connection process between the ground plane 30 and the passive components 14 (i.e., a high temperature soldering process) may serve a beneficial purpose. Such a process would seal the passive components 14 in place and prevent any solder from entering vias 48 during further completion of the circuit's construction. Preventing the introduction of additional solder into vias 48 is important, as it should be noted that unlike the vias of Figures 1 and 2, the walls of vias 48 are not conductive thus preventing any connectivity problems with the circuitry. Under certain circumstances, the epoxy material forming the various laminea 22, 24 and 26 can be made to flow and seal in the edges of the components 14 in the vias 48. This would prevent any subsequent solder from running down the sides of the vias 48 and shorting out the component.

Still further, the lands 18 are generally designed utilizing a thick-film technique to allow for the components 12 and 14 to be soldered in their normal configuration. With the presently preferred embodiment, the use of thin-film terminations on the ends of the components 12 and 14 would still allow reliable and sufficient electrical connection by way of a typical lower temperature solder connection and would be preferred due to their reduction in the cost of manufacturing of the PCB 10 and its associated circuitry.

Figure 5 provides an enlarged view of an exemplary passive component 14 as mounted in a via 48 in accordance with the present invention. As can be seen,

the passive component 14 is electrically connected to the ground plane 30 by way of either a solder or conductive epoxy material 62. The remainder of the open area in the via 48 may be filled with a non-conductive filler material 51 or under certain circumstances the material constituting exemplary non-conductive layer 22 may be made to partially melt and flow into the via 48 to partially seal it. Finally, connecting the upper portion of the passive component 14 to its respective land 18 creates the top conductor 64.

In still a further preferred embodiment of the present invention, Figures 6-13 shows the use of a blind via 148 to house electrically connected intermediate components 114 within an integrated passive device 150. In such an embodiment, the vias 148 contain various passive components 114 as discussed above which serve in addition to their electrical functions as connections between other of the passive components comprising the device 150. In this manner, the footprint of an IPD may be reduced while providing greater flexibility in its design layout.

In particular, the two non-conductive layers 152 and 154 of the IPD shown in Figures 6 and 7 represent the basic skeletal construction of an exemplary IPD. The first non-conductive layer 152, as shown in Figure 6, is a typical multilayer green ceramic pad with various circuitry and capture pads 156 on an upper surface thereof. The capture pads 156 are for electrical connection to other components within the device 150. Figure 7 shows the second such non-conductive layer 154 with a plurality of vias 148 drilled therethrough. In particular, each via 148 corresponds to a respective capture pad 156 from the first non-conductive layer 152.

As can be seen in Figure 8, the second layer 154 is bonded to the upper

surface of the first layer 152 embedding the circuitry thereon in between the layers 152 and 154. The vias 148 however, allow electrical connection to such circuitry by way of the capture pads 156. In bonding the two layers 152 and 154 together, it should be noted that any of a number of known methods may be used to make the layers 152 and 154 an essentially unitary body 150, including: lamination, weight-firing, spritzing a solvent or using the slip as glue.

With the basic construction of the device's skeletal form 150 completed, as can be seen in Figure 9, the manufacturer is now able to form the additional resistive/conductive patterns 158 required on an outer surface of the device and band terminate the edges to provide points of electrical connection 160 for such device. The methods of making such patterns 158 and terminations 160 are varied but generally known in the art. They form no particular aspect of the present invention and therefore will not be explained in detail.

Figure 10 depicts the inclusion of the internal passive components 114 into the vias 148 to provide the electrical connection between the embedded circuitry on the first layer 152 and that on the outer surface of the device 150. Each passive component 114 will be pre-selected for its performance characteristics and will ultimately be permanently embedded within the vias 148. To provide a stable electrical connection with their respective capture pads 156, the lower end of each passive component may be dipped in either a solder paste or a conductive epoxy 162 which is either cured or through the technique of reflow permanently affixed to the contact pad 156 thus forming the bottom contact for the passive component 114. Figure 11 shows the passive components 114 located within their respective vias 148.

In order to ensure both the electrical and physical stability of the passive component 114, the vias 148 may be filled with an insulating epoxy 166 or other similar material to partially encase the passive component 114 and hold it in place. As discussed above and as seen in Figure 12, if the conductor patterns have been formed either by thin-film plating or thick-film printing, the electrical connection to the upper conductor 164 may then be formed by filling in the remaining portion of the via 148 either with a conductor or a solder paste and either cure or reflow it, respectively.

Alternatively, if the upper conductors 164 for electrical connection to the via-located passive components 114 have not yet been formed, the manufacturer may choose to screen the conductors 164 and allow the excess material to flow into the remaining space in the partially filled vias 148 to generate the electrical connection between the passive components 114 and the upper conductors 164.

As does Figure 5, Figure 13 provides an enlarged view of a via-located passive component 114 as mounted in an IPD 150. As before, the passive component 114 is permanently affixed to its respective capture pad 156 through the use of either a solder or conductive epoxy material 162 and then the manufacturer either reflows or cures it, respectively. An insulating epoxy 166 may then be used as a filler material in the via 148 to partially seal it. Finally, the passive component 114 may be electrically connected to the upper conductors 164 as described above.

Although multiple preferred embodiments of the invention have been described using specific terms and devices, such description is for illustrative

purposes only. The words used are words of description rather than of limitation. It is to be understood that changes and variations may be made by those of ordinary skill in the art without departing from the spirit or the scope of the present invention, which is set forth in the following claims. In addition, it should be understood that aspects of various other embodiments may be interchanged both in whole or in part. Therefore, the spirit and scope of the appended claims should not be limited to the description of the preferred versions contained herein.

19. A multi-layer electronic device comprising:

a first device layer with a first series of resistive/conductive patterns thereon;

a second device layer with a plurality of via drilled therethrough;

a unitary device body formed by the bonded union of the first and second device layers, wherein each of said via correspond to a respective capture pad in said first series of resistive/conductive patterns;

a second series of resistive/conductive patterns on an outer layer of said unitary body;

a plurality of terminations on said unitary body for electrical connection between other electronic devices and components of said device;

individual passive components vertically mounted into each of said plurality of via and bonded to its respective capture pad; and

an electrical connection between each of said passive components and at least a portion of said second series of resistive/conductive patterns on said outer surface of said unitary device body.

20. The multi-layer electrical device of claim 19, wherein said first and second layers are made of FR4.

21. The multi-layer electrical device of claim 20, where said device is a printed circuit board.

22. The multi-layer electrical device of claim 19, wherein said first and second layers are made of a non-conductive ceramic.

23. The multi-layer electrical device of claim 23, wherein said device is an integrated passive component.

24. The multi-layer electrical device of claim 19, wherein said passive components comprise any combination of resistors, capacitors, varistors, and thermistors.

25. A multi-layer electronic device comprising:

a plurality of first device layers, each such layer having a first series of resistive/conductive patterns thereon and a plurality of via drilled therethrough;

a plurality of second device layers, each such layer having a plurality of via drilled therethrough;

a unitary device body formed by the bonded union of an interleaved stack of said plurality of first and said second device layers, wherein each of said via correspond to a respective portion of the resistive/conductive patterns on the underlying device layer and wherein one of said second device layers forms the uppermost device layer and the lowermost device layer is one of said first device layers;

a second series of resistive/conductive patterns on an outer layer of said uppermost device layer;

a plurality of terminations on said unitary body for electrical connection between other electronic devices and various of the resistive/conductive patterns throughout said unitary device body;

individual passive components vertically mounted into each of said plurality of via and electrically connected to a portion of said underlying first device layer's first series of resistive/conductive patterns; and

an electrical connection between each of said passive components and at least a portion of said overlying first device layer's first series of resistive/conductive patterns through a corresponding one of said first device layer's plurality of via.

ABSTRACT OF THE DISCLOSURE

A method of using blind via to house electronic components within an electrical device is provided. Such a method allows for the vertical orientation of various types of passive components within a layer of a printed circuit board (PCB) or an integrated passive device (IPD). One exemplary embodiment of the method provides for the passive component's electrical connection between an embedded ground and another device on the surface of the PCB. By virtue of its component positioning, such a method reduces the space demands placed upon the surface of the PCB, enhances the flexibility of circuitry design, and allows for a greater variety of passive components and integral passive devices to be utilized within the PCB itself. Another exemplary embodiment of the method provides for greater flexibility in the design and manufacture of IPDs by allowing for the vertical electrical connection of various passive components through the placement of intervening passive components into via.

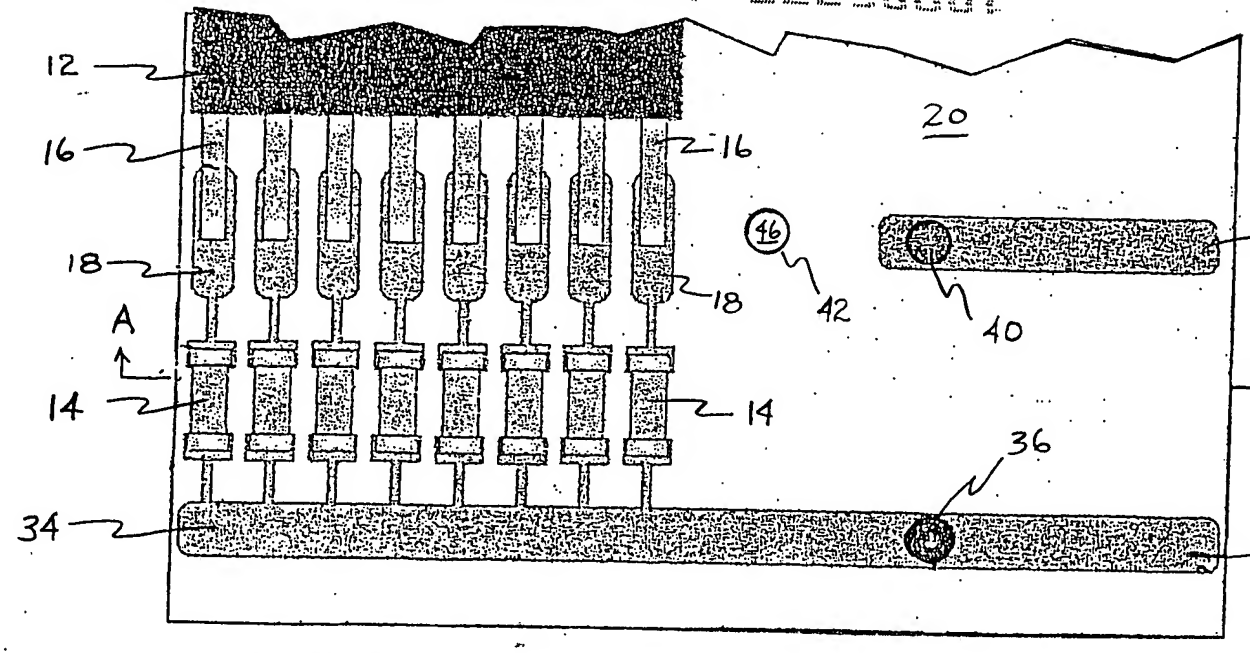
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FIG 1

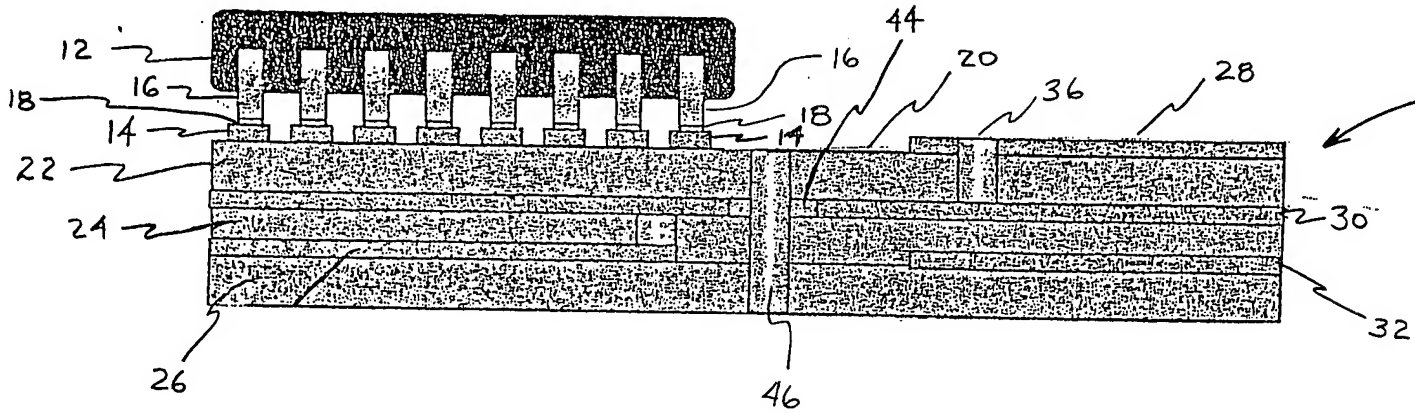
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FIG 2

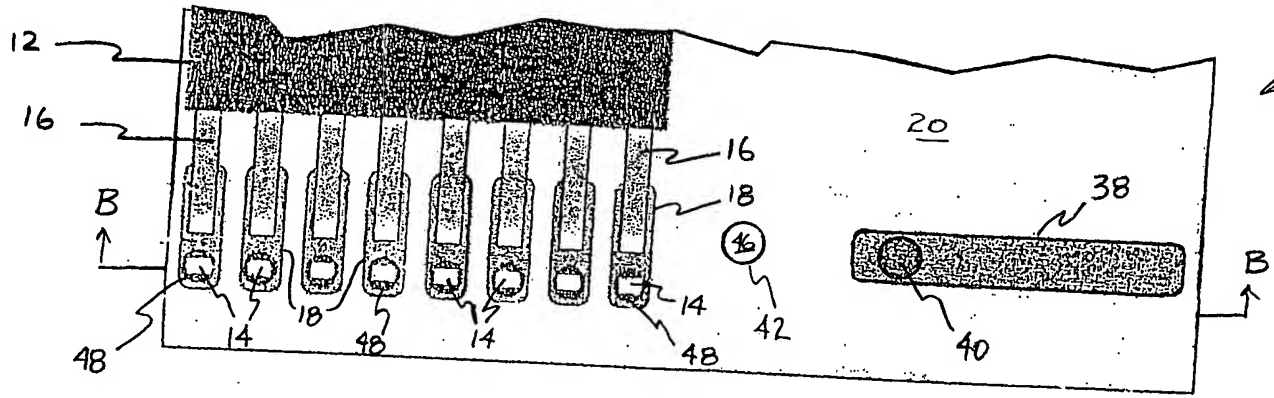

FIG. 3

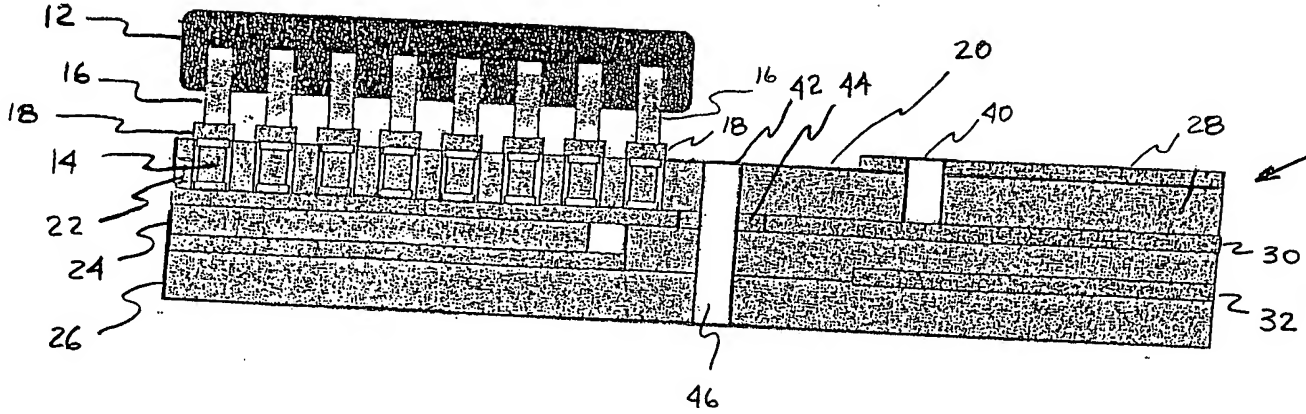

FIG. 4

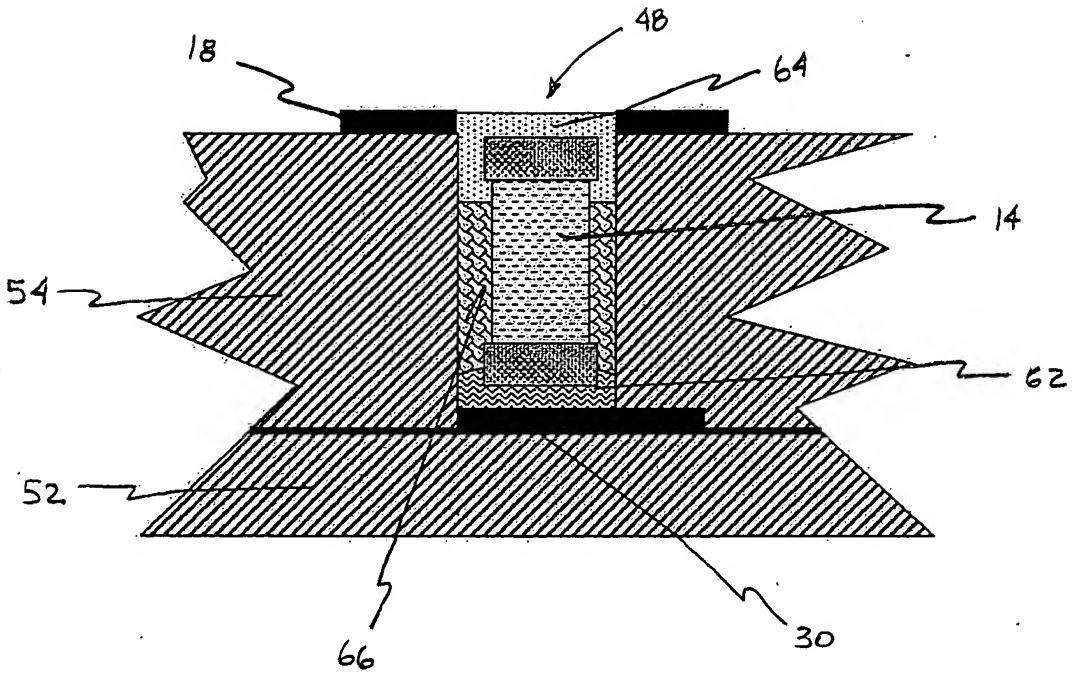

Figure 5

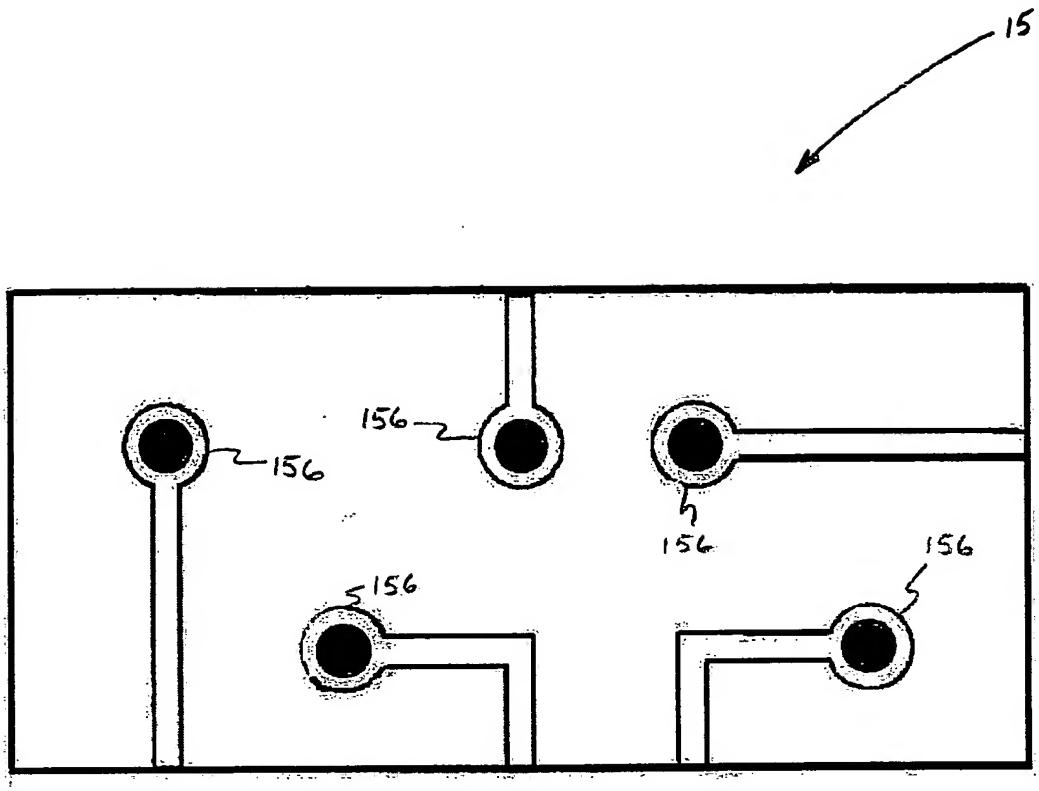

Figure 6

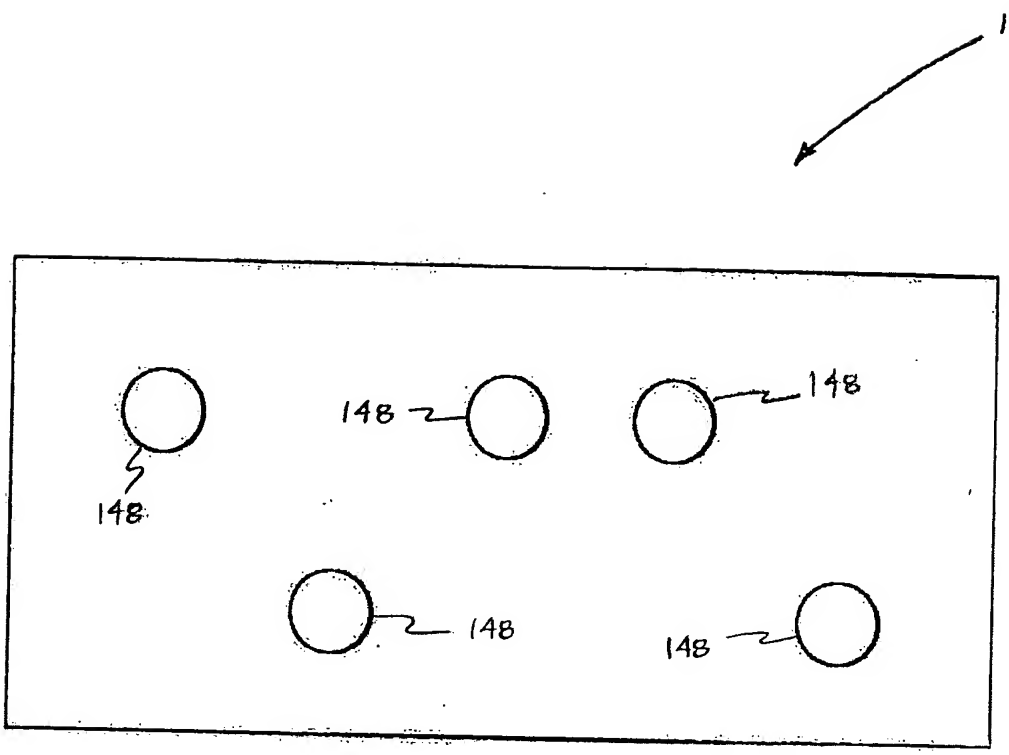

Figure 7

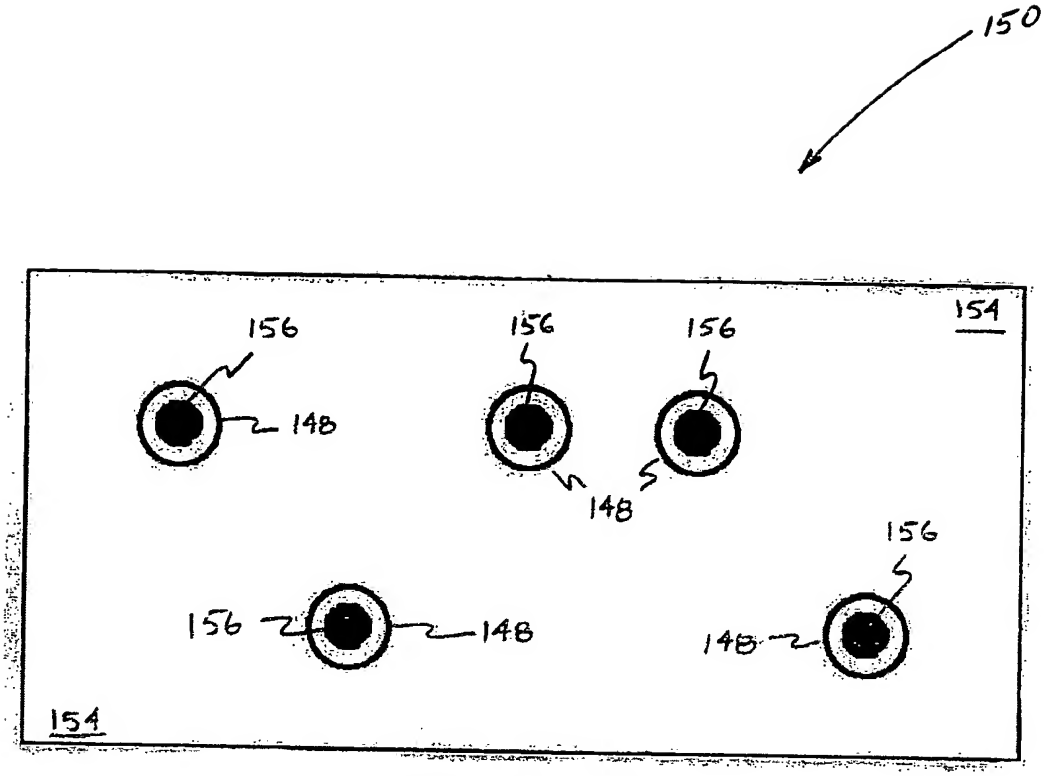

Figure 8

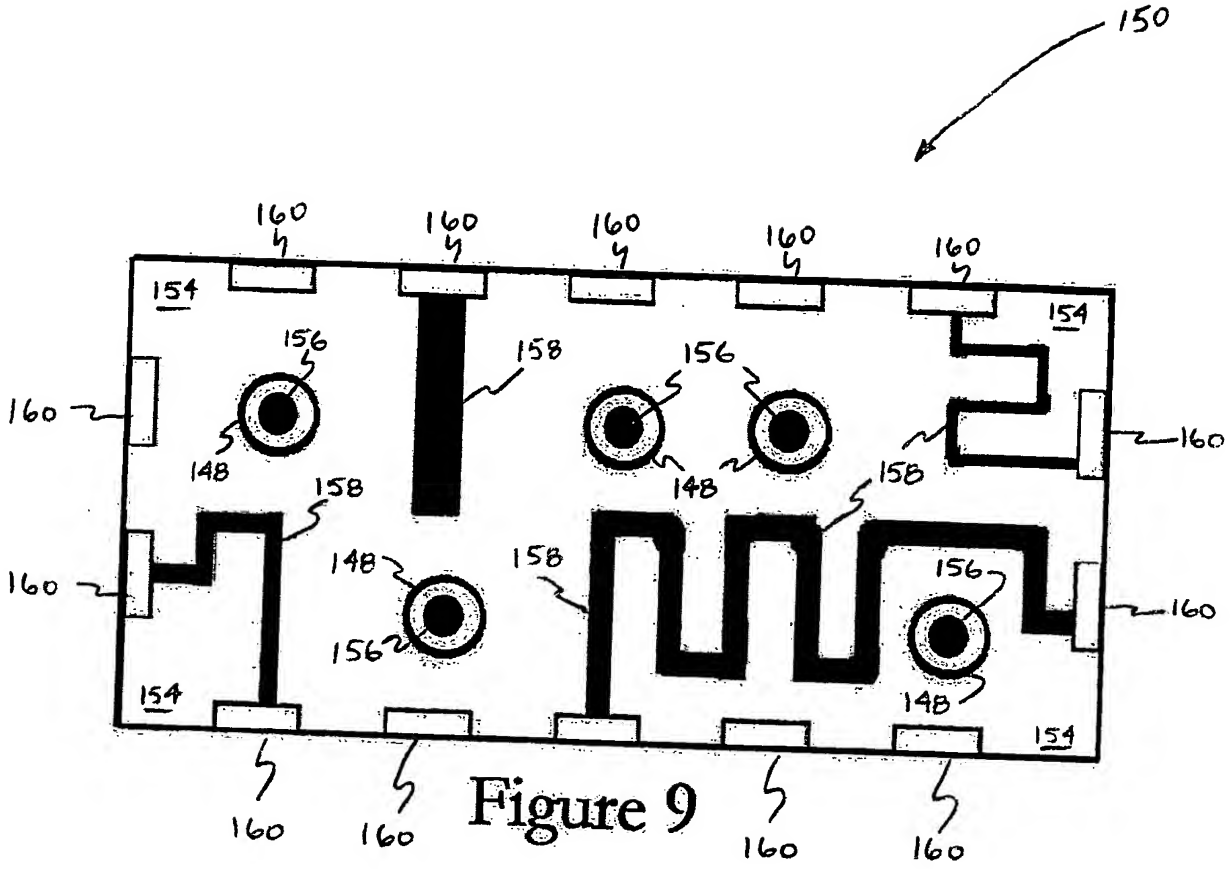

Figure 9

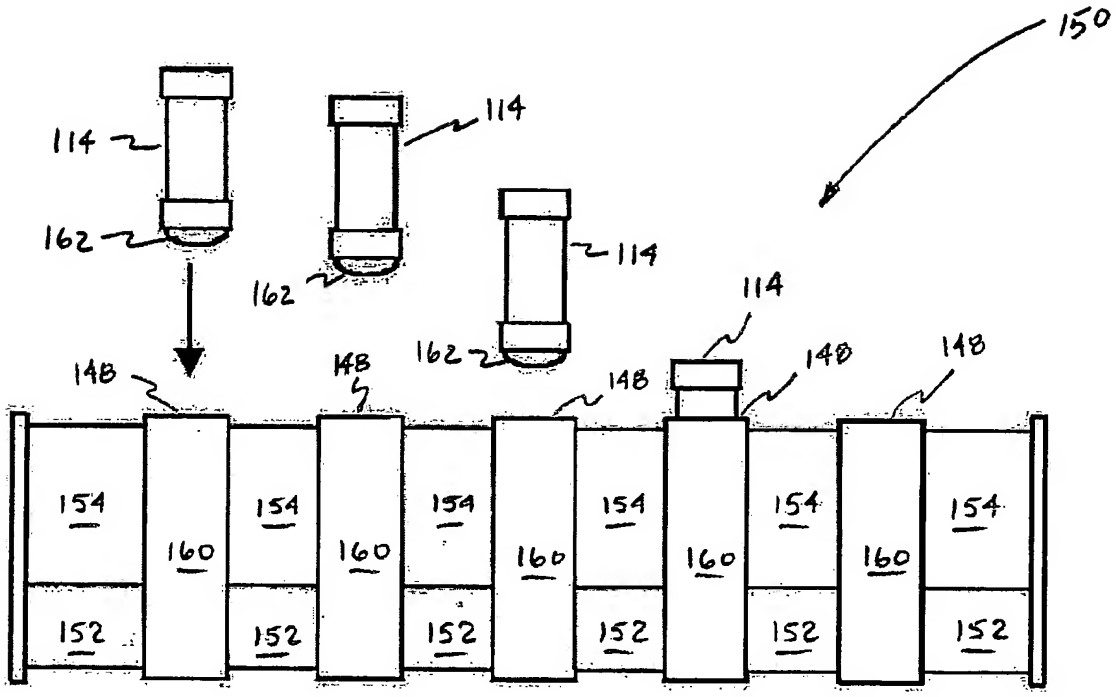
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Figure 10

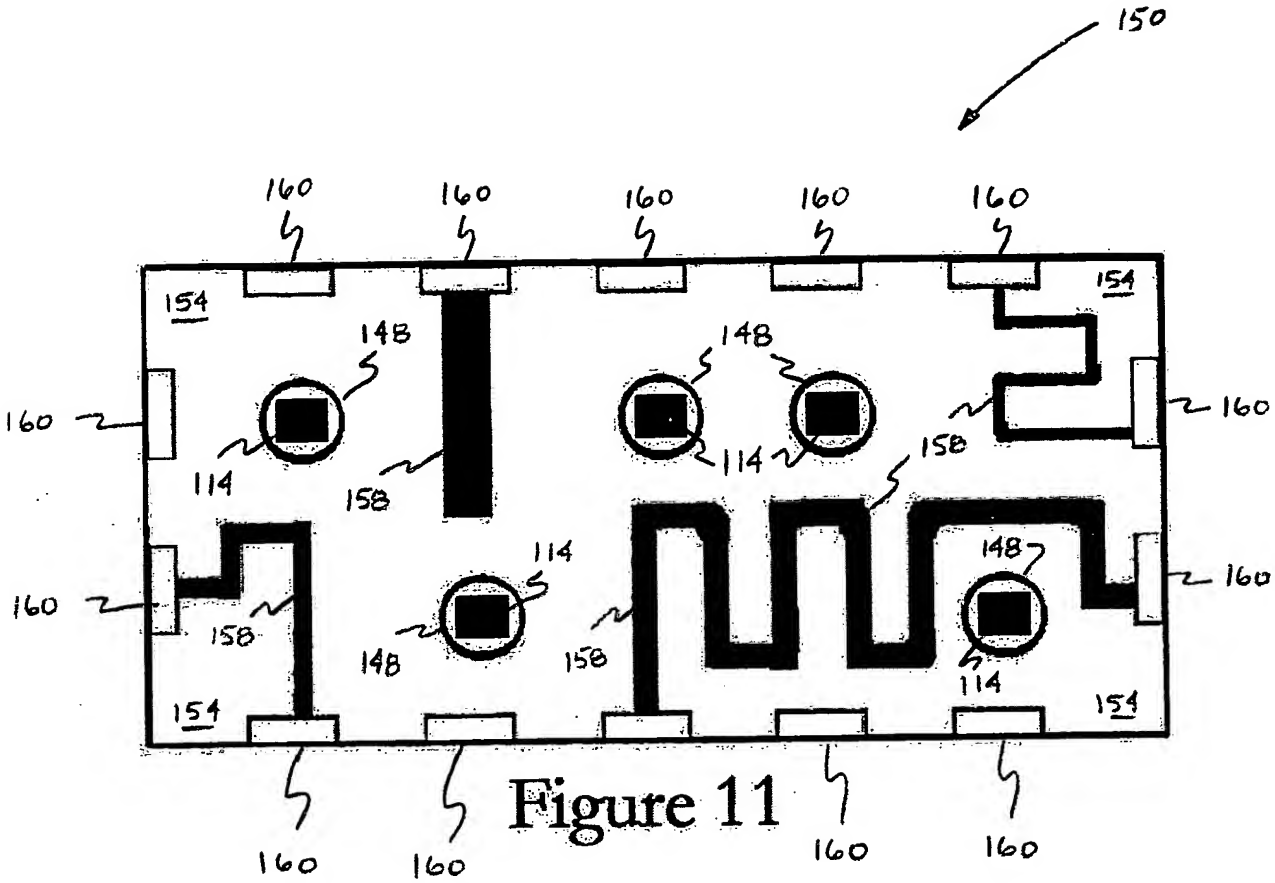
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Figure 11

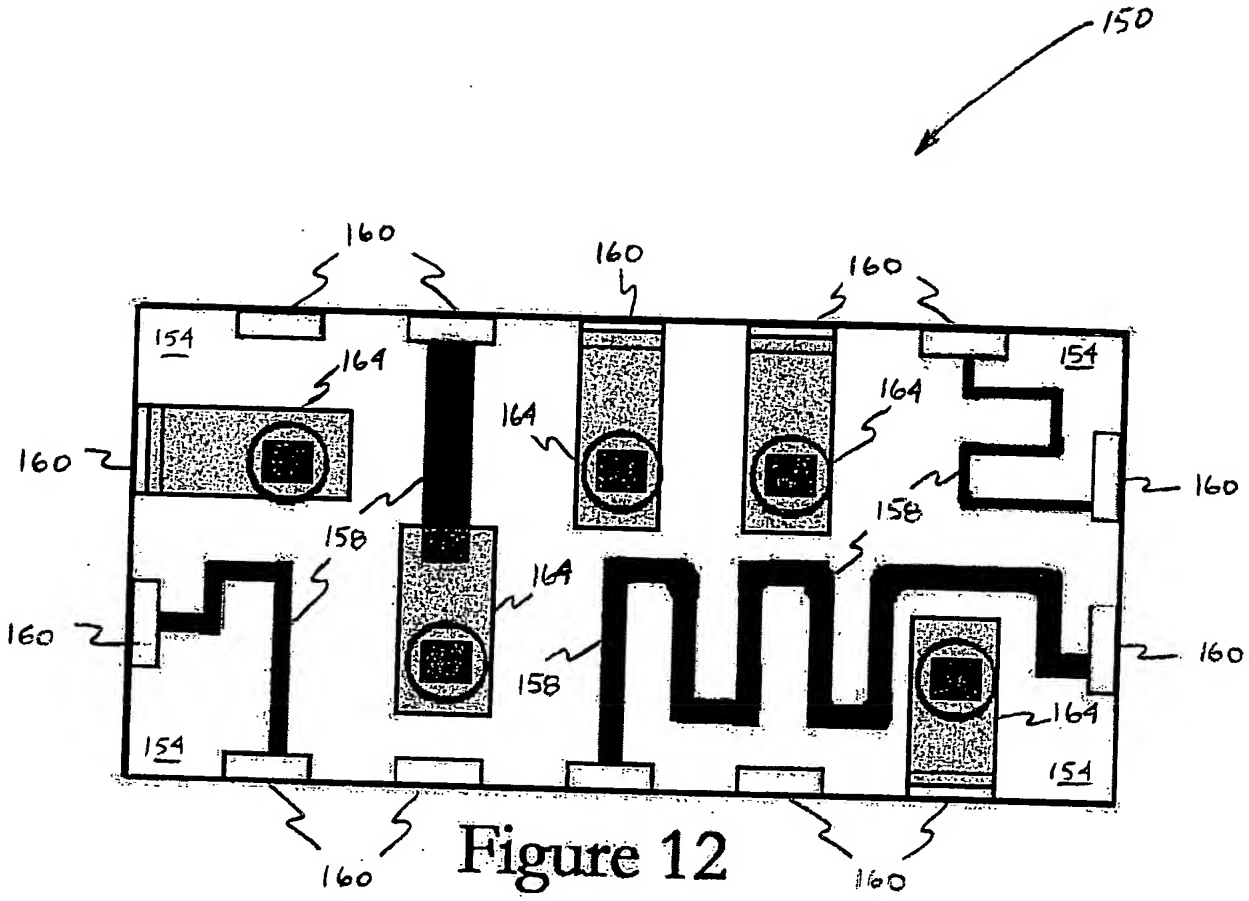
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Figure 12

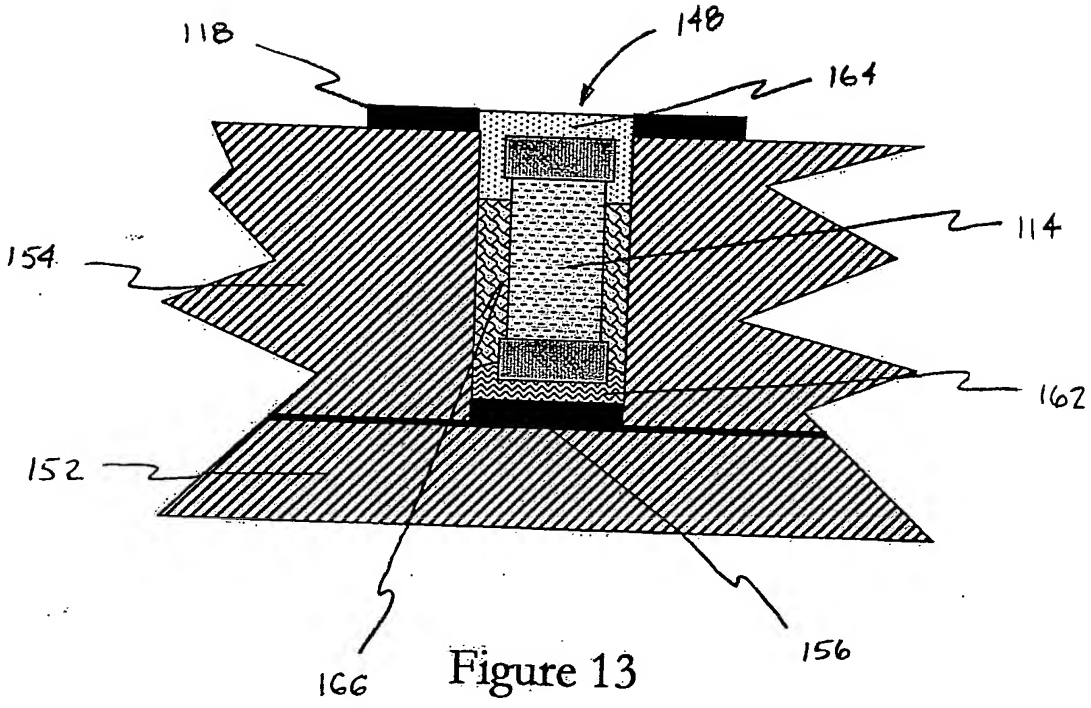

Figure 13

FILE 'WPIX, JAPIO'

L1 59 S RESISTIVE(W) CONDUCTIVE

L2 63 S RESISTIVE(W) CONDUCTIV?

L3 202708 S ELECTRIC?(2N)(CONNECT? OR JOIN? OR BOND?)

L4 157 S FR4 OR FLAME(W) RETARDANT(W)(4 OR FOUR OR IV)

L5 137057 S (MOTHER OR CIRCUIT)(W) BOARD OR MOTHERBOARD OR CIRCUITBOARD

L6 31995 S S01-G01B/MC OR G01R-031/28/IC

L7 284 S NON(W) CONDUCT?(2N) CERAMIC OR NONCONDUCT?(2N) CERAMIC

L8 845 S PASSIVE(W) COMPONENT

L9 902946 S VIA

L10 36 S L4 AND ((L5 OR L6))

L11 0 S L4 AND L7

L12 0 S L4 AND L8

L13 0 S L4 AND L2

L14 166435 S (L5 OR L6)

L15 166399 S L14 NOT L10

L16 2 S L15 AND L2

L17 3 S L15 AND L7

L18 93 S L15 AND L8

L19 23 S L18 AND L3

L20 551 S RESISTIVE(2N) CONDUCTIV?

L21 32 S L15 AND L20

L22 28 S L16 OR L17 OR L19

L23 29 S L21 NOT (L22 OR L10)

L24 5 S L20 AND L8

L25 1 S L24 NOT (L22 OR L10 OR L21)

L26 0 S (GALVAGNI, JOHN L OR GALVAGNI, JOHN L OR GALVAGNI, JOHN L OR GALVAGNI, JOHN L)/AU

L27 5 S (GALVAGNI JOHN L OR GALVAGNI, JOHN L OR GALVAGNI, J L OR GALVAGNI J L)/AU

L28 12 S (GALVAGNI JOHN OR GALVAGNI, JOHN OR GALVAGNI, J OR GALVAGNI J)/AU

L29 17 S (L27 OR L28) NOT (L22 OR L10 OR L21 OR L24)

L30 153321 S ELECTR?(W)(DEVICE OR CIRCUIT)

L31 153303 S L30 NOT (L10 OR L22 OR L21)

L32 3 S L31 AND L4

L33 3 S L31 AND L2

L34 10 S L31 AND L7

L35 63 S L31 AND L8

L36 14652 S L31 AND L3

L37 11 S L35 AND L3

L38 27 S L32 OR L33 OR L34 OR L37

L10 ANSWER 1 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2002-740675 [80] WPIX
DNN N2002-583601 DNC C2002-209652
TI Sub-lamination layer for use in electronic components used in computer, pager, has single layer etched reference plane in between signal layers using adhesives.
DC A85 L03 P73 V01 V04
IN OHR, S S; OHR, S
PA (OHRS-I) OHR S S; (HONE) HONEYWELL INT INC
CYC 92
PI WO 2002054845 A2 20020711 (200280)* EN 20p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
US 2002122923 A1 20020905 (200280)
ADT WO 2002054845 A2 WO 2001-US49183 20011218; US 2002122923 A1 US 2000-752538 20001228
PRAI US 2000-752538 20001228
AB WO 200254845 A UPAB: 20021212
NOVELTY - The top and bottom surfaces of a single layer etched reference plane made of copper or nickel are formed in between signal films using adhesives such as cyanate ester.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for:
(1) electronic component;
(2) Sub lamination layer production method; and
(3) electronic component production.
USE - Sub lamination layer for use in electronic components such as capacitor, inductor and resistor and **circuit board** chip packaging and keyboard used in commercial electronic products such as television, computer, cellular phone, pager, palm-type organizer, portable radio, car stereo, remote control, etc.
ADVANTAGE - Avoids need for the metal and dielectric layers for each signal layer pair, thereby reduces the cost and the size of the Sub lamination layer.
Dwg.0/4

L10 ANSWER 2 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2002-566172 [60] WPIX
DNN N2002-448255 DNC C2002-160339
TI Folded flexible **circuit board** for Kinestatic Charge Detector, has lower rigid portion, lower and upper foldable strips with diagonal folding lines, intermediate portions, and connector board.
DC A85 L03 V04
IN JAIN, J J; LAUGHTER, J; SAMANT, S S
PA (SJUD-N) ST JUDE CHILDREN'S RES HOSPITAL; (UYTE-N) UNIV TENNESSEE RES CORP
CYC 1
PI US 2002075660 A1 20020620 (200260)* 21p
US 6483713 B2 20021119 (200280)
ADT US 2002075660 A1 US 2001-989626 20011120; US 6483713 B2 US 2001-989626 20011120
PRAI US 2001-989626 20011120
AB US2002075660 A UPAB: 20020919
NOVELTY - A folded flexible circuit comprise lower rigid portion, lower and upper foldable strips with diagonal folding lines, intermediate portion(s) with a circuit pattern connected to opposite ends of the strips, and a connector board connected to an opposite end of the upper

strip.

DETAILED DESCRIPTION - A folded flexible circuit comprises a lower rigid portion having a circuit pattern, lower foldable strip(s) having a circuit pattern at one end for connection to the circuit pattern of the lower rigid portion (210), intermediate portion(s) having a circuit pattern with a first end connected to an opposite end of the foldable strip, upper foldable strip(s) having a circuit pattern electrically connected at a second end intermediate portion (230), and a connector board electrically connected to an opposite end of the upper foldable strip. The connector board receives connectors to provide external attachment to the **circuit board**. The lower and upper foldable strips include diagonal folding lines arranged so that the foldable strips fold in opposite directions of each other.

INDEPENDENT CLAIMS are included for the following:

(1) A Kinestatic Charge Detector comprising a tubular chamber and the inventive folded **circuit board** in the chamber;and

(2) A process for manufacturing the inventive folded flexible **circuit board**.

USE - For use in Kinestatic Charge Detector.

ADVANTAGE - The invention is more compact and has a much greater ratio of open area to folded area to be usable in devices where space is limited or overall a reduction in size is desired. It increases reliability, weight and space savings, reduced mechanical connectors, and has greater impedance control.

DESCRIPTION OF DRAWING(S) - The figure shows the **circuit board** device.

Lower rigid portion 210

Intermediate portion 230

Dwg.6/9

L10 ANSWER 3 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2002-488186 [52] WPIX
DNN N2002-385800
TI Manufacture of coated synthetic bodies, e.g. optical disks, involves pretreatment in excited gas atmosphere of noble gas and nitrogen and/or hydrogen, and limiting ion energy of the excited gas.
DC P42
IN CHEN, M; HAN, C; WANG, P; XIAO, R
PA (HEAD-N) HEADWAY TECHNOLOGIES INC
CYC 1
PI US 6383574 B1 20020507 (200252)* 6p
ADT US 6383574 B1 US 1999-360118 19990723
PRAI US 1999-360118 19990723
AB US 6383574 B UPAB: 20020815

NOVELTY - Coated synthetic bodies are manufactured by subjecting a surface of the bodies to a pretreatment in an atmosphere of excited gas formed of a noble gas and nitrogen and/or hydrogen. The ion energy of ions of the excited gas on the surface to be coated is limited to at most 50 eV. The pre-treated surface is then coated.

USE - For manufacturing coated synthetic bodies, e.g. optical disks, optical components, printed **circuit boards** or components for semiconductor manufacturing.

ADVANTAGE - The inventive method can be easily perform which includes a storage time of the pretreated synthetic surfaces in a normal atmosphere. It provides good coating adhesion on the synthetic surface.

DESCRIPTION OF DRAWING(S) - The figure shows a system for implementing pretreatment within the framework of the production process of the coated synthetic bodies.

Dwg.1/1

L10 ANSWER 4 OF 36 WPIX (C) 2003 THOMSON DERWENT

AN 2002-470679 [50] WPIX
DNN N2002-371549 DNC C2002-133773
TI Grid interposer for use with integrated circuit components comprises planar insulating layer including orienting features, and conductive pad(s) comprising upper and lower pad bodies joined by connecting bars.
DC L03 S01 V04
IN CLAYTON, G A
PA (CLAY-I) CLAYTON G A
CYC 1
PI US 2002039847 A1 20020404 (200250)* 16p
ADT US 2002039847 A1 Provisional US 2000-238197P 20001004, US 2001-912111 20010723
PRAI US 2000-238197P 20001004; US 2001-912111 20010723
AB US2002039847 A UPAB: 20020807
NOVELTY - Grid interposer comprises a planar insulating layer including orienting features and defining several vias, and at least one conductive pad comprising upper and lower pad bodies joined by connecting bars which extend through the vias and are contiguous with the upper and lower pad bodies.

DETAILED DESCRIPTION - Grid interposer comprises a planar insulating layer (12) including orienting features (24) and defining several vias through the insulating layer, and at least one conductive pad comprising upper and lower pad bodies (26, 28) joined by connecting bars (34) which extend through the vias and are contiguous with the upper and lower pad bodies. Each of the upper and lower pad bodies includes contact posts extending away from the insulating layer. The conductive pads provide electrical contact with an integrated circuit (IC) component in contact with the contact posts of the upper pad body and with an IC component in contact with the contact posts of the lower pad body by penetration of an oxidation layer on the IC components by the contact posts. The grid interposer is placed in a contact position by the use of the orienting features of the planar insulating layer.

An INDEPENDENT CLAIM is also included for a method of making a grid interposer for use with integrated circuit components, which comprises enclosing an insulating layer between an upper and a lower conductive layer; adding photoresist layers to the exterior surfaces of the upper and lower conductive layers; selectively removing the photoresist layers from at least one first defined region and from at least one corresponding second defined region, so that the photoresist layers are selectively removed from the exterior surface of the upper and the lower conductive layer only within the first defined regions of the upper conductive layer and within the corresponding second defined regions of the upper conductive layer; forming vias within the first and second defined regions which penetrate the upper conductive layer, the inner insulating layer, and the lower conductive layer; filling the vias with a layer of conductive material, forming connecting bars of conductive material which penetrate the insulating layer and which electrically connect the upper and the lower conductive layers, and which also forms a first pad body on the upper conductive layer and a second pad body on the lower conductive layer, within each of the first and second defined regions; cutting valley profiles in the first and the second pad bodies which form by isolation several contact posts from each of the first and second pad bodies; adding a conductive metallic layer to the upper and lower conductive layers and the contact posts; removing the photoresist layer from the upper conductive and the lower conductive layers; removing the upper and the lower conductive layers outside the first and the defined regions to expose the insulating layer; and forming at least one orienting feature in the insulating layer for aiding in positioning the grid interposer in use.

USE - The grid interposer is used with integrated circuit components. It is used for testing electrical circuits and for establishing electrical connection between components.

ADVANTAGE - The invention creates a contact surface which will cut through the oxidation layer of the conductive metals, form a clean and predictable electrical connection with ICs pads, will last a long time, and which will not damage electrodes. It forms a solderless interchangeable connection.

DESCRIPTION OF DRAWING(S) - The figure is a perspective view of the grid interposer.

Insulating layer 12
Orienting features 24
Upper and lower pad bodies 26, 28
Connecting bars 34

Dwg.1/5

L10 ANSWER 5 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2002-444664 [47] WPIX
DNN N2002-350281
TI Inverted F-antenna suitable for integration in mass-produced products.
DC W02
IN ALPASLAN, A; HOPF, B P; KALAYCI, Y
PA (SIEI) SIEMENS AG
CYC 20
PI WO 2002043186 A1 20020530 (200247)* DE 32p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: US
DE 10058863 A1 20020620 (200248)
ADT WO 2002043186 A1 WO 2001-DE4456 20011127; DE 10058863 A1 DE 2000-10058863 20001127
PRAI DE 2000-10058863 20001127
AB WO 200243186 A UPAB: 20020725
NOVELTY - An antenna has a resonant body (AAA) with a first electrical connection point (AS) to a feed point (SP) on a printed circuit module (**FR4**) and a second connection (SS) to the ground connection point (MP) on the module. The first connection from the resonant body (AA) to the feed point (SP) is especially a push-fit wire. Also claimed is an antenna (A') which is an inverted F antenna formed entirely by a push-fit wire which links a first contact hole in the feeding point (SP') and the second contact hole in the ground collection point (MP').

USE - Transceiver aerial.

ADVANTAGE - The aerial combines compact dimensions and enhanced tolerance to printed **circuit board** contact points. No trap ribs are required to secure the antenna. The aerial is suitable for integral use in conjunction with mass-produced products.

DESCRIPTION OF DRAWING(S) - The drawing shows an inverted F-antenna with a transverse radiator made of bent wire. (Drawing includes non English-language text).

Dwg.2/5

L10 ANSWER 6 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2002-436611 [47] WPIX
DNN N2002-343625 DNC C2002-124214
TI Arrangement, used as card of sensor, has **circuit board** with regions separated by slit-like recess which terminates inside **circuit board** and extends up to moisture-impermeable barrier layer.
DC A89 J04 S02 S03 V04
IN GEHRKE, M; PECHSTEIN, T
PA (ENDR) ENDRESS & HAUSER CONDUCTA GES MESS; (GEHR-I) GEHRKE M; (PECH-I) PECHSTEIN T
CYC 27
PI DE 10052532 A1 20020502 (200247)* 5p
EP 1204301 A2 20020508 (200247) DE

R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
US 2002139573 A1 20021003 (200267)
DE 10052532 C2 20021114 (200277)
ADT DE 10052532 A1 DE 2000-10052532 20001023; EP 1204301 A2 EP 2001-124306 20011019; US 2002139573 A1 US 2001-1668 20011023; DE 10052532 C2 DE 2000-10052532 20001023
PRAI DE 2000-10052532 20001023
AB DE 10052532 A UPAB: 20020725
NOVELTY - An arrangement for forming a switch for receiving and processing an electrical signal has a switch arranged on a **circuit board** (4). A first region (2) of the **circuit board** supporting the switch is separated from a second region surrounding the first region by a slit-like recess (10) which terminates inside the **circuit board** and extends up to a moisture-impermeable barrier layer. The recess and the first region are cast using a moisture-impermeable casting composition (24).
DETAILED DESCRIPTION - Preferred Features: The barrier layer is a metallic layer (18). The **circuit board** is formed from a **FR4** material which has a moisture-impermeable barrier layer inside. The walls (26) of the **circuit board** limiting the recess are provided with a moisture-impermeable coating.
USE - Used as a card of a measuring value processing device, especially a sensor (claimed).
ADVANTAGE - Moisture is prevented from contacting the switch.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section through the **circuit board**.
First region of **circuit board** 2
Circuit board 4
Slit-like recess 10
Metallic layer 18
Casting composition 24
Walls of **circuit board** 26
Dwg.2/2

L10 ANSWER 7 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2002-415504 [44] WPIX
DNN N2002-326860 DNC C2002-117273
TI Carrier for land grid array connector, comprises multiple cylindrical openings provided in carrier structure each of which is electrically conductive and positioned to accept contact structure.
DC A85 U11 V04
IN FAN, Z; LE, A D; LI, C
PA (HIGH-N) YIGH CONNECTOR DENSITY INC; (FANZ-I) FAN Z; (LEAD-I) LE A D; (LICC-I) LI C; (HIGH-N) HIGH CONNECTION DENSITY INC
CYC 4
PI WO 2002017435 A2 20020228 (200244)* EN 38p
W: CN JP KR
US 2002098721 A1 20020725 (200254)
US 6471525 B1 20021029 (200274)
KR 2002042712 A 20020605 (200277)
ADT WO 2002017435 A2 WO 2001-US25431 20010814; US 2002098721 A1 Provisional US 2000-227859P 20000824, Div ex US 2001-772641 20010130, US 2002-73589 20020212; US 6471525 B1 Provisional US 2000-227859P 20000824, US 2001-772641 20010130; KR 2002042712 A KR 2002-704603 20020410
PRAI US 2001-772641 20010130; US 2000-227859P 20000824; US 2002-73589 20020212
AB WO 200217435 A UPAB: 20020711
NOVELTY - A carrier for land grid array connectors comprises: (a) a carrier structure (42) that has layer(s) of dielectric material on the surface(s) of which a shielding layer (57) is arranged; and (b) multiple

cylindrical openings (50) provided in the carrier structure, each of which is electrically conductive and positioned to accept a contact structure (16a).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of forming a shielded substrate structure and carrier for land grid array connectors.

USE - For land grid array connectors which interconnects electrical circuit structures such as printed **circuit board**, circuit modules which are used in information handling system or telecommunication environments.

ADVANTAGE - Achieves improved retention of conductors, manufacturability, reliability and more uniform mechanical and electrical performance.

DESCRIPTION OF DRAWING(S) - The figure shows a partial perspective view of electrical connector.

Contact structure 16a

Carrier structure 42

Openings 50

Shielding layer 57

Dwg.2a/3

L10 ANSWER 8 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2002-380531 [41] WPIX
CR 2000-159878 [14]; 2000-337947 [29]; 2000-542871 [49]; 2001-334522 [35]; 2001-449951 [48]; 2001-540813 [60]; 2002-380530 [41]; 2002-380677 [41]; 2002-403361 [43]; 2002-414214 [44]; 2002-517908 [55]
DNN N2002-297613
TI Adhesive material applying apparatus for printed **circuit board**, has stop bar provided in adhesive reservoir, to arrange a portion of lead finger at predetermined distance from pool chamber opening.
DC P42 U11
IN AHMAD, S S
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6336974 B1 20020108 (200241)* 29p
ADT US 6336974 B1 CIP of US 1997-906578 19970805, CIP of US 1997-906673 19970805, Div ex US 1998-20197 19980206, US 1998-183233 19981029
FDT US 6336974 B1 CIP of US 6013535, Div ex US 6040205
PRAI US 1998-20197 19980206; US 1997-906578 19970805; US 1997-906673 19970805; US 1998-183233 19981029
AB US 6336974 B UPAB: 20020903

NOVELTY - An adhesive reservoir (110) comprises an adhesive pool chamber having an upward opening. A stop bar (196) is provided to the adhesive reservoir, to arrange a portion of lead finger (104) at a predetermined distance from the opening of the pool chamber.

USE - For applying adhesive material such as thermoplastic, thermoset resin, flowable paste, B-stage adhesive material on printed **circuit board**, **FR4**, for mounting semiconductor chip using direct chip attach (DCA) technique and also on semiconductor die for integrated circuit used by computer industry.

ADVANTAGE - Since stop bar is provided to adhesive reservoir, the need for highly accurate adhesive material control system is eliminated and the depth of immersion of lead finger into the adhesive material, is also limited.

DESCRIPTION OF DRAWING(S) - The figure shows a side cross-sectional view explaining the method of applying adhesive material using stop bar.

Lead finger 104

Adhesive reservoir 110

Stop bar 196

Dwg.32/53

L10 ANSWER 9 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2002-207750 [27] WPIX
DNN N2002-158389 DNC C2002-063589
TI Manufacture of flip-chip assembly for mounting large chips on substrates, e.g. printed **circuit board**, involves using isotropically conductive adhesive and non-conductive material in the same assembly cycle.
DC A85 L03 U11
IN STOUKACH, S; VANDECASTEELE, B; VANFLETEREN, J
PA (INTE-N) INTERUNIV MICRO-ELEKTRONICA CENT VZW; (INTE-N) INTERUNIV MICRO-ELECTRONICA CENT VZW
CYC 27
PI EP 1126517 A2 20010822 (200227)* EN 18p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
JP 2001298052 A 20011026 (200227) 50p
ADT EP 1126517 A2 EP 2001-870022 20010209; JP 2001298052 A JP 2001-34244 20010209
PRAI US 2000-181402P 20000209
AB EP 1126517 A UPAB: 20020429
NOVELTY - An apparatus, e.g. flip-chip assembly, is produced by providing a substrate (3) and a component (1); dispensing and drying an isotropically conductive adhesive (6) on bonding pads of either the substrate or of the component; applying an underfill material (5) between the bonding pads of the substrate; and exerting a mechanical pressure on the aligned component.

DETAILED DESCRIPTION - Manufacture of an apparatus, i.e. flip-chip assembly, involves providing a substrate and a component, each of which comprising bonding pads or contact pads (2b); dispensing an isotropically conductive adhesive (ICA) on the bonding pads of either the substrate or of the component; drying the ICA; applying an underfill material, that is a non-conductive adhesive (NCA), between the bonding pads of the substrate; aligning the component so that the bonding pads of the component are directly above the bonding pads of the substrate; and exerting a mechanical pressure on the component until a predetermined distance between the component and the substrate is reached. The bonding pads of the component and the substrate are contacting with the ICA. Curing is performed while maintaining the mechanical pressure and the predefined distance. A thermocompression step is performed to cure the ICA and NCA, thus creating electrical contacts between the component and the substrate.

USE - For manufacturing an apparatus, e.g. flip-chip assembly, for mounting large chips with high input/output count or small pitch, on substrates, e.g. printed **circuit board** (PCB). The PCB assemblies are used in telecommunications.

ADVANTAGE - The process is simplified, reliable, and cost-effective. It is applicable in all types of substrates including cheap, or low-temperature substrates. The flip-chip assemblies produced can withstand reflow soldering, ICA curing and even wave soldering.

DESCRIPTION OF DRAWING(S) - The figures are process sequences of forming the flip-chip assembly.
Component 1
Bonding pads or contact pads 2b
Substrate 3
Underfill 5
Adhesive 6
Tool 8
4E, 4F/8

L10 ANSWER 10 OF 36 WPIX (C) 2003 THOMSON DERWENT

AN 2002-099061 [14] WPIX
DNC C2002-031028
TI Metal coating application onto a plastic product, in particular optical data storage discs and printed **circuit boards**, involves pretreatment in a gas atmosphere.
DC A35 A85 L03 M13
IN BECK, E; RAMM, J; ZIMMERMANN, H
PA (BALV) UNAXIS BALZERS AG
CYC 27
PI EP 1156131 A1 20011121 (200214)* DE 9p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
US 6383573 B1 20020507 (200238)#
ADT EP 1156131 A1 EP 2001-111533 20010511; US 6383573 B1 US 2000-572089 20000517
PRAI CH 2000-983 20000517; US 2000-572089 20000517
AB EP 1156131 A UPAB: 20020301
NOVELTY - Prior to coating the product surface is pretreated in a chamber(11) with an exited gas atmosphere comprising a rare gas and nitrogen and/or hydrogen. Ion energy in the gas and close to the substrate surface is not more than 50eV.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is made for a use for the process in the manufacture of optical data storage discs, optical lenses, printed **circuit boards** or parts for semi-conductor production.
USE - For coating optical data storage discs, optical lenses, printed **circuit boards** or parts for semi-conductor production(All claimed).
ADVANTAGE - The process can be used as a standard process, is independent of the plastic surface to be coated and/or coating material and ensures good adhesion between the coating material and plastics which can be difficult to coat, e.g. PMMA.
DESCRIPTION OF DRAWING(S) - The drawing shows a plant scheme for the pretreatment process.
pretreatment chamber 11
Dwg.1/1

L10 ANSWER 11 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2002-096530 [13] WPIX
DNN N2002-071266 DNC C2002-029933
TI Carrier for land grid array connectors, comprises adhesive layer provided between upper and lower sections of substrate.
DC A85 L03 V04
IN FAN, Z; LE, A D; LI, C
PA (HIGH-N) YIGH CONNECTOR DENSITY INC; (HIGH-N) HIGH CONNECTION DENSITY INC; (FANZ-I) FAN Z; (LEAD-I) LE A D; (LICC-I) LI C
CYC 4
PI US 6312266 B1 20011106 (200213)* 15p
WO 2002017393 A1 20020228 (200222) EN
W: CN JP KR
KR 2002038761 A 20020523 (200274)
ADT US 6312266 B1 US 2000-645860 20000824; WO 2002017393 A1 WO 2001-US25407 20010814; KR 2002038761 A KR 2002-703640 20020319
PRAI US 2000-645860 20000824
AB US 6312266 B UPAB: 20020226
NOVELTY - A carrier (42) for land grid array connectors comprises a substrate having upper and lower sections (44, 46) and openings (50) positioned to accept a contact element (16). An adhesive layer (48) is provided intermediate the upper and lower sections, and is contacting portion(s) of the contact element to provide improved retention.
USE - The carrier is used for local grid array (LGA) connectors for

interconnecting at least two electrical circuit members, e.g. printed **circuit boards** or circuit modules. The LGA connectors can also be used in information handling system (e.g., computer), telecommunications network device, handheld personal digital assistant, or medical equipment.

ADVANTAGE - The carrier provides improved retention of the individual contact elements. It is employed in LGA interposer connectors exhibiting improved manufacturability, reliability, and more uniform electrical and mechanical performance. It is less expensive to manufacture and can be easily assembled.

DESCRIPTION OF DRAWING(S) - The figure shows a side section of the LGA connector.

Contact element 16

Carrier 42

Upper and lower sections 44, 46

Adhesive layer 48

Openings 50

Spacers 52, 54

Alignment openings 56

Dwg.2b/4

L10 ANSWER 12 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2002-068296 [10] WPIX
DNN N2002-050567 DNC C2002-020576
TI Electroless plating of semiconductor chips, involves attaching chip(s) having bonding pads to carrier using pressure sensitive adhesive, electroless plating the bond pads, and detaching chip(s) from the carrier.
DC A85 L03 P42 U11
IN DE PAUW, H; VAN FLETEREN, J; ZHANG, S; PAUW, H D; VANFLETEREN, J
PA (INTE-N) INTERUNIV MICRO-ELECTRONICA CENT VZW; (UYGE-N) UNIV GENT; (PAUW-I) PAUW H D; (VANF-I) VANFLETEREN J; (ZHAN-I) ZHANG S
CYC 27
PI EP 1156521 A2 20011121 (200210)* EN 18p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
US 2002001670 A1 20020103 (200210)
ADT EP 1156521 A2 EP 2001-870087 20010424; US 2002001670 A1 Provisional US 2000-199421P 20000424, US 2001-841359 20010424
PRAI US 2000-199421P 20000424; US 2001-841359 20010424
AB EP 1156521 A UPAB: 20020213
NOVELTY - Electroless plating of semiconductor chips involves attaching the chip(s) having bonding pads to a carrier using a pressure sensitive adhesive. The bond pads are then electroless plated, and the chip(s) is detached from the carrier.

USE - The method is used for electroless plating of semiconductor chips.

ADVANTAGE - The method provides uniform plate bonding pads on singulated chips, single dice, wafer parts or wafer in a much more simple and cost-effective manner.

Dwg.0/9

L10 ANSWER 13 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2001-496631 [54] WPIX
DNN N2001-368029
TI An array of electrical connectors for high frequency integrated circuit chips and board level connections includes an array of plated through receptacle holes having land pads with overhanging flanges to receive and engage pins.
DC U11 V04
IN KORHONEN, M A; LI, C; SHI, W
PA (HIGH-N) HIGH CONNECTION DENSITY INC

CYC 3
PI WO 2001045212 A1 20010621 (200154)* EN 30p
W: CN JP KR
ADT WO 2001045212 A1 WO 2000-US3843 20000215
PRAI US 1999-461064 19991214
AB WO 200145212 A UPAB: 20010924
NOVELTY - A printed **circuit board** (40) has an array of receptacle holes (14) into which low-cost cylindrical pins (10) are inserted and engaged. The pin may have an alternative cross-section and may be tapered to assist insertion. The **circuit board** is made of a core (32) of glass-epoxy composite, such as **FR4**, and includes copper or copper alloy grounding layers (41, 42), traces (44) and plated through hole walls (25) with land pads (22) having overhanging flanges (22a).

USE - The array of electrical connectors is used for high frequency integrated circuit chips and board level connections.

ADVANTAGE - The overhanging flanges serve as bending beams of spring-like contact elements. The connectors are small enabling high density and room for compensating capacitive components, reduce cross-talk and coupling noise, and allow low-cost short pins to maintain a low profile connection.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an electrical connector.

Pin 10
Receptacle hole 14
Land pad 22
Flange 22a
Through hole wall 25
Core 32
Printed **circuit board** 40
Grounding layers 41, 42
Trace 44
Dwg.2a/3

L10 ANSWER 14 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2001-409919 [44] WPIX
DNN N2001-303132
TI Manufacturing method for electrical resistance inserted into **circuit-board** especially multilayer **circuit board** - involves making boring into **circuit-board** and them introducing resistance paste into boring to form contact with electrical conductor.
DC U11 U14 V01 V04
IN GRASSER, E; KATZIER, H
PA (SIEI) SIEMENS AG
CYC 1
PI DE 10015269 A1 20010628 (200144)* 6p
ADT DE 10015269 A1 DE 2000-10015269 20000328
PRAI DE 2000-10015269 20000328
AB DE 10015269 A UPAB: 20010809
A method of manufacturing an electrical resistance for placing within a **circuit-board** (e.g. a multi-layer **circuit-board**) involves initially introducing a boring into a **circuit-board** (**FR4**-ML) and then placing resistance paste (WP) in the boring in such a way that the paste each time forms a contact with an electrical conductor in different layers of the **circuit-board**.

A further **circuit-board** layer is specifically pressed on to the **circuit-board**. More specifically, a further **circuit-board** layer is pressed on to both sides of the **circuit-board**, and the resistance paste

makes contact with a conductor arranged between two layers.
USE - Complex electronic circuits, such as integrated circuits.
ADVANTAGE - Reduced parasitic interference.
Dwg.1a-d/3

L10 ANSWER 15 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2001-356276 [38] WPIX
CR 2001-147655 [01]
DNN N2001-258907
TI PCB dipole antenna configuration, e.g. for cellular telephones and data links, includes a matching network and dipole elements etched on opposite sides of a printed **circuit board**.
DC V04 W01 W02 W07
IN CHEN, X; GUO, Y; ZHU, L
PA (SUPE-N) SUPERPASS CO INC
CYC 1
PI CA 2307515 A1 20001028 (200138)* EN 28p
ADT CA 2307515 A1 CA 2000-2307515 20000428
PRAI CA 1999-2270302 19990428
AB CA 2307515 A UPAB: 20010711
NOVELTY - A single element printed dipole antenna (10) includes a matching network (3) of a pair of printed strips and a patch (4) extending from a feed connection (1) etched on opposite sides of a standard **FR4** PCB (2). U-shaped dipole elements are formed on either side of the PCB with bases (5, 6) having a narrow gap between their edges (5a, 6a). Strips form a printed dipole antenna on the left side (7A, 8A) and on the right side (7B, 8B).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a printed circuit antenna including antenna elements formed on one substrate and feed elements formed on a second substrate.
USE - The printed antenna configuration is used for a dipole antenna in commercial and military applications of cellular telephones and data links.
ADVANTAGE - Common mode currents are minimized thus reducing antenna performance degradation. The antenna is easily manufactured, uses a standard **FR4** PCB, is low in cost and small in size and achieves improved gain.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic top view of a dipole antenna configuration.
Feed connection 1
PCB 2
Matching network 3
Patch 4
Bases of dipole elements 5, 6
Edges 5a, 6a
Strips of dipole elements 7A, 7B and 8A, 8B
Dwg.1/10

L10 ANSWER 16 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2001-348587 [37] WPIX
DNN N2001-252531 DNC C2001-108113
TI Composite magnetic substance for inhibiting electromagnetic interference in electronic machines such as portable telephone, personal computers, comprises flame retardant, soft magnetic powder and binder.
DC L03 V02 W02
PA (TOHM) TOKIN CORP
CYC 1
PI JP 2001085212 A 20010330 (200137)* 6p
ADT JP 2001085212 A JP 1999-257459 19990910
PRAI JP 1999-257459 19990910
AB JP2001085212 A UPAB: 20010704

NOVELTY - The composite magnetic substance (CMS) (1) comprises soft magnetic powder (3), binder (2) and **flame retardant (4)**. The flame retardant contains inorganic compound and/or inorganic hydroxide.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the electromagnetic interference inhibition material.

USE - For inhibiting the interference of unnecessary electromagnetic wave in high frequency area of electronic machines such as portable telephones and personal computers.

ADVANTAGE - Thin shaped CMS is light in weight and effectively reduces electromagnetic interference between electronic components and **circuit boards**, and prevents generation of unnecessary electromagnetic waves. The CMS excels in flame retardant property, shields noise production, prohibits usage of choke or filter in noise transmission lines and improves self extinguishing property. The CMS shortens ignition time after autolysis, thereby reducing burning time and evolution of harmful gas during disposition of electrical equipments.

DESCRIPTION OF DRAWING(S) - The figure shows the cross sectional view of composite magnetic substance.

Composite magnetic substance 1

Binder 2

Soft magnetic powder 3

Flame retardant 4

Dwg.1/1

L10 ANSWER 17 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2001-217330 [22] WPIX
CR 2000-255458 [18]
DNN N2001-154826
TI Plastic ball grid array injection solder mold for mounting integrated circuits onto printed **circuit boards**, includes at least one double chamfered through-hole with width similar to its height.
DC U11 V04 X24
IN BOLDE, L R; GRUBER, P A; LEI, C C
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6153505 A 20001128 (200122)* 7p
ADT US 6153505 A Div ex US 1998-67904 19980427, US 1999-388300 19990901
FDT US 6153505 A Div ex US 6029882
PRAI US 1998-67904 19980427; US 1999-388300 19990901
AB US 6153505 A UPAB: 20010421
NOVELTY - The mold comprises two major surfaces penetrated and connected by at least one double chamfered through-hole (2). The width of the through-hole is equal to its height. The mold is comprised by material which is substantially non-wettable by the solder.

DETAILED DESCRIPTION - The coefficient of thermal expansion of the material of mold is similar to that of the substrate onto which the solder is transferred. The material of mold is either graphite, **FR4** resin laminate or its combination.

USE - For mounting the ICs onto laminated PCBs, and packaging of integrated circuits.

ADVANTAGE - The combination of non-wettability of the mold material, the double chamfers and the aspect ratio of the mold through-holes, facilitates the solder balls to form and release cleanly during reflow. Since the mold is made of non-wettable material, the solder balls adhere to the substrate without leaving solder residue within the walls of the mold through-holes. Thus, clean mold can be reused easily. Since the coefficient of thermal expansion of the mold material is similar to that of the substrate, the solder balls are transferred to the PCB in the desired places and the mold material will not crack during solder transfer.

DESCRIPTION OF DRAWING(S) - The figure represents the cross-sectional side view of the through-hole of the PBGA mold after reflow.
Through-hole 2
Dwg.2B/3

L10 ANSWER 18 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2001-158659 [16] WPIX
DNN N2001-115595 DNC C2001-046993
TI Laminate for multilayer printed **circuit board**, includes inner substrate made of phenolic resin laminated paper.
DC A85 L03 P73 V04
IN NOVAL, J V; SPRIETSMA, J T
PA (ITLC) INTEL CORP
CYC 1
PI US 6180215 B1 20010130 (200116)* 10p
ADT US 6180215 B1 US 1999-353310 19990714
PRAI US 1999-353310 19990714
AB US 6180215 B UPAB: 20010323
NOVELTY - Insulating layer (3) of prepreg material is formed on either sides of laminated inner substrates (107) made of phenolic resin laminated paper. A copper foil layer (5) is formed on outer surfaces of the insulating layer, as the outer layer of laminate.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) a multilayer printed **circuit board**; and
(b) a laminate manufacturing process.
USE - For multilayer printed **circuit board** used in mounting IC chips.
ADVANTAGE - The phenolic resin laminated paper is less expensive than inner core fiber glass reinforced epoxy resin (**FR4**) material, hence cost of multilayer substrate board is reduced.
DESCRIPTION OF DRAWING(S) - The drawing shows the schematic sectional view of 6-layer stack-up for multilayer PCB.
insulating layer 3
copper foil layer 5
inner substrate 107
Dwg.4/7

L10 ANSWER 19 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2001-147655 [16] WPIX
CR 2001-356276 [01]
DNN N2001-108181
TI A printed antenna configuration for a dipole antenna in commercial and military applications of cellular telephones and data links includes a matching network and dipole elements etched on opposite sides of a printed **circuit board**.
DC W02
IN CHEN, X; GUO, Y; ZHU, L
PA (SUPE-N) SUPERPASS CO INC
CYC 2
PI CA 2270302 A1 20001028 (200116)* EN 18p
US 6377227 B1 20020423 (200232)
ADT CA 2270302 A1 CA 1999-2270302 19990428; US 6377227 B1 US 2000-559530 20000428
PRAI CA 1999-2270302 19990428
AB CA 2270302 A UPAB: 20020521
NOVELTY - A single element printed dipole antenna (10) includes a matching network (3) of a pair of printed strips and a patch (4) extending from a feed connection (1) etched on opposite sides of a standard **FR4** printed **circuit board** (PCB) (2). U-shaped dipole elements are formed on either side of the PCB with bases (5, 6) having a

narrow gap between their edges (5a, 6a). Strips form a printed dipole antenna on the left side (7A, 8A) and on the right side (7B, 8B).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a printed circuit antenna including antenna elements formed on one substrate and feed elements formed on a second substrate.

USE - The printed antenna configuration is used for a dipole antenna in commercial and military applications of cellular telephones and data links.

ADVANTAGE - Common mode currents are minimized thus reducing antenna performance degradation. The antenna is easily manufactured, uses a standard **FR4** PCB, is low in cost and small in size and achieves improved gain.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic top view of a dipole antenna configuration.

Feed connection 1

PCB 2

Matching network 3

Patch 4

Bases of dipole elements 5, 6

Edges 5a, 6a

Strips of dipole elements 7A, 7B and 8A, 8B

Dwg.1/7

L10 ANSWER 20 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2000-504895 [45] WPIX
DNN N2000-373279 DNC C2000-151477
TI Surface-mountable fuse for protection against electrical overload on printed **circuit boards**, has fusible link with diffusion bar of different conductive materials, containment compound and terminal pads.
DC A85 L03 X13
IN FRITZ, S E; MINERVINI, A; RESTIS, T
PA (LITF) LITTELFUSE INC
CYC 1
PI US 6078245 A 20000620 (200045)* 6p
ADT US 6078245 A US 1998-213193 19981217
PRAI US 1998-213193 19981217
AB US 6078245 A UPAB: 20000918

NOVELTY - A surface-mountable fuse comprises a fusible link of a first conductive material and having a diffusion bar of a second conductive material, a containment compound covering a portion of the diffusion bar and extends into a substrate adjacent to the fusible link, and a pair of terminal pads.

DETAILED DESCRIPTION - A surface-mountable fuse comprises:

(1) a fusible link (12) of a first conductive material supported on a substrate (13) and having a diffusion bar (18) of a second conductive material along a section of the link;

(2) a containment compound (20) deposited over a portion of the fusible link and covers a portion of the diffusion bar and extends into the substrate adjacent to the fusible link; and

(3) a pair of terminal pads (14, 16) formed on the substrate and electrically connected to the link.

Under electrical overload conditions the link will blow at or near the diffusion bar and the compound inhibits migration of the diffusion bar along the fusible link.

USE - For protection against electrical overload on printed **circuit boards**.

ADVANTAGE - The invention exhibits improved control of fusing characteristics by regulating voltage drop across the fusible link. Restriking tendencies are minimized by selection of an optimized material for the substrate, the containment compound and the protective layer. The

invention provides desired arc-tracking characteristics and exhibits sufficient mechanical flexibility to remain intact when exposed to the rapid release of energy associated with arcing.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the fuse.

Fusible link 12

Substrate 13

Terminal pads 14, 16

Diffusion bar 18

Containment compound 20

Dwg.3/3

L10 ANSWER 21 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2000-292354 [25] WPIX
DNN N2000-219261 DNC C2000-088198
TI Production of treated metallic foil comprises electrodepositing a dusty dendritic metal and a uniform metal flash over the dendritic deposit for use in electronic devices.
DC L03 M11 U21 V04 X13
IN SADEY, R J; ZATT, D M
PA (GOUN) GOULD ELECTRONICS INC
CYC 1
PI US 6042711 A 20000328 (200025)* 7p
ADT US 6042711 A Cont of US 1993-22797 19930223, US 1997-920405 19970829
PRAI US 1993-22797 19930223; US 1997-920405 19970829
AB US 6042711 A UPAB: 20000524

NOVELTY - Production of treated metallic foils having an improved peel strength comprises (A) electrodepositing a dusty dendritic metal deposit and (B) electrodepositing a uniform metal flash over the dendritic deposit of (A).

DETAILED DESCRIPTION - Production of treated metallic foil having an improved peel strength comprises: (A) electrodepositing a dusty dendritic layer of copper on one surface of a metal foil with a current density of 250-400 amperes per square foot, a copper ion concentration of 24-26 g/l, a bath temperature of 90-110 deg. F and a sulfuric acid concentration of 90-110 g/l; and (B) electrodepositing on the surface of the dusty dendritic deposit of step (A) a uniform metal flash major amount of a metal other than copper to provide a treated metallic foil exhibiting a peel strength of at least 12 pounds per inch based upon GI-**FR4** lamination.

USE - For the manufacture of metal foil used in various electronic and electrical devices e.g. printed **circuit board** (PCB) and PCB components specially multilayer PCB laminates, solid state switches and solid state circuit breakers.

ADVANTAGE - The metallic foil produced has an improved peel strength and capable of enduring thermochemical stress and reduced treatment transfer.

Dwg.0/3

L10 ANSWER 22 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2000-255458 [22] WPIX
CR 2001-217330 [05]
DNN N2000-189840 DNC C2000-077875
TI Solder injection mold for attaching solder balls to printed **circuit board** has chamfered through holes receiving molten solder from reservoir on one side and transferring it to board in the form of balls on being reflowed.
DC A85 L03 V04 X24
IN BOLDE, L R; GRUBER, P A; LEI, C C
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 2

PI US 6029882 A 20000229 (200022)* 7p
CA 2302907 A1 20010929 (200169)# EN
ADT US 6029882 A US 1998-67904 19980427; CA 2302907 A1 CA 2000-2302907 20000329
PRAI US 1998-67904 19980427; CA 2000-2302907 20000329
AB US 6029882 A UPAB: 20011126
NOVELTY - Double chamfered through holes (2) in a solder injection mold are filled with molten solder (9) from a reservoir (5) at one major surface while a base plate (4) is applied to a second major surface. After cooling the solder, a substrate (6) is placed against the second surface with mounted components (7) positioned within blind recesses (3) of the mold and contact lands aligned with the chamfered openings and the solder is reflowed to contract into solder balls (8) which attach themselves to the lands.

DETAILED DESCRIPTION - Preferred Features: The solder injection molding tool is made of material having the same coefficient of thermal expansion as that of the material from which the substrate is made. Both materials are made from graphite and/or **FR4** resin laminate. The solder is eutectic. Each chamfered through hole includes a straight-walled portion connecting the chamfered openings. The aspect ratio of the holes, i.e., ratio of depth to unchamfered width, is preferably 3:4 - 1:2.

USE - For packaging integrated circuits by mounting them onto laminated printed **circuit boards** by means of solder balls using a plastic ball grid array (PBGA) technique.

ADVANTAGE - The mold enables the solder balls to be attached to a printed **circuit board** in a controlled and reliable fashion. The mold and base plate are reusable for processing a large number of boards.

DESCRIPTION OF DRAWING(S) - The figures show the through holes in the injection mold being filled with solder and the solder being reflowed for transfer to the printed **circuit board**.

Double-chamfered through-holes 2
blind recess for accommodating electronic component 3
base plate 4
molten solder reservoir 5
substrate or printed **circuit board** 6
solder balls 8
solder in hole 9
Dwg.3B,3E/3

L10 ANSWER 23 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 2000-097445 [08] WPIX
DNN N2000-075307
TI Anisotropic conductive adhesive application for mounting flip-chip on PCB.
DC V04
IN KANG, R; ZHONG, Z
PA (GINT-N) GINTIC INST MFG TECHNOLOGY; (SIEI) SIEMENS AUDIOLOGISCHE TECH GMBH
CYC 82
PI WO 9963794 A1 19991209 (200008)* EN 19p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
AU 9876834 A 19991220 (200021)
ADT WO 9963794 A1 WO 1998-SG40 19980602; AU 9876834 A AU 1998-76834 19980602, WO 1998-SG40 19980602
FDT AU 9876834 A Based on WO 9963794
PRAI WO 1998-SG40 19980602

AB WO 9963794 A UPAB: 20000215
NOVELTY - The anisotropic conductive adhesive (1), e.g. a thermoplastic, is coated on the surface of a printed **circuit board** (PCB) (2). An active surface (5) of a die (3) is fixed on the PCB, covering the adhesive. Heat is applied to the adhesive and force is applied between the die and the PCB. The contacts (7) on the die are connected to the corresponding contacts on the PCB by adhesive.

DETAILED DESCRIPTION - The PCB has a ceramic or **FR4** substrate.

USE - For applying anisotropic conductive adhesive for mounting semiconductor chips or flip-chips on PCBs.

ADVANTAGE - Facilitates installation of the die on the PCB using only one adhesive. Facilitates removal of a defective die for exchange with a new die by just melting the adhesive.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the installation of a die on a PCB.

Anisotropic conductive adhesive 1
PCB 2
Die 3
Active surface 5
Contact 7
Dwg.4/12

L10 ANSWER 24 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 1999-494948 [42] WPIX
DNN N2000-144903 DNC C2000-060869
TI Paste for capping electrodes comprises unzippable polymer, a suitable solvent and particles of gold and/or tin.
DC A13 A17 A85 L03 U11 V04 X12
IN COTTE, J M; ROLDAN, J M; SAMBUCETTI, C J; SARAF, R F
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 2
PI CN 1219741 A 19990616 (199942)*
US 6013713 A 20000111 (200018)B 10p
US 6221503 B1 20010424 (200125)
US 6281105 B1 20010828 (200151)
ADT CN 1219741 A CN 1998-123832 19981104; US 6013713 A US 1997-965227 19971106; US 6221503 B1 Div ex US 1997-965227 19971106, US 1999-382400 19990824; US 6281105 B1 Div ex US 1997-965227 19971106, US 1999-382401 19990824
FDT US 6221503 B1 Div ex US 6013713; US 6281105 B1 Div ex US 6013713
PRAI US 1997-965227 19971106; US 1999-382400 19990824; US 1999-382401 19990824
AB US 6013713 A UPAB: 20000412 ABEQ treated as Basic
NOVELTY - Paste for forming a conductive coating on a C4 bump containing lead (Pb) and tin (Sn) comprises a solvent for an unzippable polymer comprising poly(alpha -methyl styrene), polypropylene carbonate, polyethylene carbonate or polychloral, and particles of gold (Au), tin or Au/Sn alloy suspended in the solution.

DETAILED DESCRIPTION - A paste for forming a conductive coating on a C4 bump containing lead (Pb) and tin (Sn) comprises:

(i) a solvent for an unzippable polymer;

(ii) an unzippable polymer comprising poly(alpha -methyl styrene) (PAMS), poly(propylene carbonate), poly(ethylene carbonate) or poly(chloral) dissolved in the solvent to form a solution; and

(iii) particles comprising gold (Au), tin or Au/Sn alloy suspended in the solution.

The conductive coating has a conductivity greater than 1 ohm-cm. Particles form a first alloy with Pb or Sn, that melts at 150-400 deg. C. Unzippable polymer comprises 10 wt.% or more of the solution.

USE - Paste is used for capping electrodes in low temperature

interconnections between an integrated chip and a substrate, and for coating and testing integrated circuit chips, e.g. **FR4** printed **circuit boards**. Assemblies are used in computers, office equipment, automobiles, trucks, control systems, cellular telephones, etc.

ADVANTAGE - Method is low cost.

1A-1C/10

AB CN 1219741 A UPAB: 20000419

NOVELTY - Paste for forming a conductive coating on a C4 bump containing lead (Pb) and tin (Sn) comprises a solvent for an unzippable polymer comprising poly(alpha -methyl styrene), polypropylene carbonate, polyethylene carbonate or polychloral, and particles of gold (Au), tin or Au/Sn alloy suspended in the solution.

DETAILED DESCRIPTION - A paste for forming a conductive coating on a C4 bump containing lead (Pb) and tin (Sn) comprises:

(i) a solvent for an unzippable polymer;

(ii) an unzippable polymer comprising poly(alpha -methyl styrene) (PAMS), poly(propylene carbonate), poly(ethylene carbonate) or poly(chloral) dissolved in the solvent to form a solution; and

(iii) particles comprising gold (Au), tin or Au/Sn alloy suspended in the solution.

The conductive coating has a conductivity greater than 1 ohm-cm. Particles form a first alloy with Pb or Sn, that melts at 150-400 deg. C. Unzippable polymer comprises 10 wt.% or more of the solution.

USE - Paste is used for capping electrodes in low temperature interconnections between an integrated chip and a substrate, and for coating and testing integrated circuit chips, e.g. **FR4** printed **circuit boards**. Assemblies are used in computers, office equipment, automobiles, trucks, control systems, cellular telephones, etc.

ADVANTAGE - Method is low cost.

1A-1C/10

L10 ANSWER 25 OF 36 WPIX (C) 2003 THOMSON DERWENT

AN 1998-582905 [49] WPIX

CR 1996-128304 [13]

DNN N1998-454136

TI Intermediate level printed **circuit board** for mounting IC components - includes solder paste screen that is deposited on conductive layer coarse pitch contacts as defined by coarse pitch openings in one stencil having pattern different from that of other stencil.

DC V04

IN HOEBENER, K G; HUBACHER, E M; PARTRIDGE, J P

PA (IBMC) INT BUSINESS MACHINES CORP; (MOTI) MOTOROLA INC

CYC 1

PI US 5825629 A 19981020 (199849)* 12p

ADT US 5825629 A Div ex US 1994-298983 19940831, Cont of US 1995-453028 19950530, US 1996-709674 19960909

FDT US 5825629 A Div ex US 5492266

PRAI US 1994-298983 19940831; US 1995-453028 19950530; US 1996-709674 19960909

AB US 5825629 A UPAB: 19981210

The board (1) includes a conductive interconnect layer with fine and coarse pitch contacts configured to connect surface mounted components of corresponding contact pitch on one surface of a dielectric structure core. Then, solder is reflowed onto conductive layer fine pitch contacts as defined by openings (19) in a stencil. The reflowed solder has origin composition of solder paste screen deposited into fine pitch openings in the stencil and has shape constrained by a reflow performed at an elevated temperature in presence of that stencil. A solder paste screen deposited on conductive layer coarse pitch contacts as defined by coarse pitch openings in another stencil.

The pattern of the coarse pitch stencil is different from the stencil

(17). The stencil (17) is removed after deposition of the solder paste screen. The fine pitch contacts formed using the stencil (17) are finer by factor of two or more than coarse pitch contacts defined by solder paste deposited using the other stencil. A set of components are affixed to select conductive layer fine pitch contacts using flux deposited on the reflowed solder. Another set of components are affixed to select conductive layer coarse pitch contacts using screen deposited solder paste.

USE - For surface mounted type flip chip devices.

ADVANTAGE - Avoids need for carrying out complex plating operation and equipment requirements. Maintains stand-off height between PCB contact and silicon die adequate to ensure reliable attachment under presence of significant difference in coefficient of thermal expansion between PCB and silicon die. Uses stencil material that exhibits potentially better match for **FR4** material boards. Maintains relative alignment and withstands at reflow temperature irrespective of selected mask material. Dwg.7,10/13

L10 ANSWER 26 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 1998-569909 [49] WPIX
DNN N1998-443524 DNC C1998-171413
TI Metallising non-conductive substrate regions especially **circuit board** hole walls - by colloid treatment, etchant treatment, electroless plating and electroplating.
DC A35 A85 L03 M11 M13 V04
IN SCHROEER, D; WOLFF, J
PA (ATOT-N) ATOTECH DEUT GMBH
CYC 23
PI DE 19740431 C1 19981112 (199849)* 7p
WO 9913696 A1 19990318 (199918) DE
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR US
EP 997061 A1 20000503 (200026) DE
R: AT CH DE DK ES FI FR GB IE IT LI NL SE
KR 2001023915 A 20010326 (200161)
JP 2001516961 W 20011002 (200172) 24p
TW 460614 A 20011021 (200248)
EP 997061 B1 20020731 (200257) DE
R: AT CH DE DK ES FI FR GB IE IT LI NL SE
DE 59805020 G 20020905 (200266)
ADT DE 19740431 C1 DE 1997-19740431 19970911; WO 9913696 A1 WO 1998-DE2694 19980904; EP 997061 A1 EP 1998-952563 19980904, WO 1998-DE2694 19980904; KR 2001023915 A KR 2000-702606 20000311; JP 2001516961 W WO 1998-DE2694 19980904, JP 2000-511345 19980904; TW 460614 A TW 1998-114610 19980903; EP 997061 B1 EP 1998-952563 19980904, WO 1998-DE2694 19980904; DE 59805020 G DE 1998-505020 19980904, EP 1998-952563 19980904, WO 1998-DE2694 19980904
FDT EP 997061 A1 Based on WO 9913696; JP 2001516961 W Based on WO 9913696; EP 997061 B1 Based on WO 9913696; DE 59805020 G Based on EP 997061, Based on WO 9913696
PRAI DE 1997-19740431 19970911
AB DE 19740431 C UPAB: 19981210
A process for metallising a substrate, which has electrically non-conductive regions, comprises treating with a precious metal colloid-containing solution, treating with a hydrogen peroxide etching solution containing not more than 0.5 mol/kg hydrogen ions and metallising the non-conductive surfaces by electroless plating and then electroplating. Preferably, the colloid solution is an aqueous acidic palladium colloid solution stabilised by an organic protective colloid; the etching solution contains 0.5-100 g/l hydrogen peroxide and 5-200 g/l phosphoric acid; and the electrolessly plated layer consists of cobalt, copper, palladium or preferably nickel, optionally in alloy form.

Also claimed is the metallisation of drilled hole walls in copper-coated **circuit boards** by the above process.

ADVANTAGE - The process allows reliable metallisation of widely differing materials (e.g. fibre-reinforced tetrafluoroethylene, glass fibre-reinforced **FR4** resin, polyimide laminate, polyamide, epoxy composite laminate, cyanate ester, polyetherimide, polyether sulphone, ceramics and glass) especially of **circuit board** hole surfaces without significant process modification and avoids the waste water disposal and toxicity problems of conventional electroless metallising processes.

Dwg.0/0

L10 ANSWER 27 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 1998-260597 [23] WPIX
CR 2000-327951 [28]
DNN N1998-205428 DNC C1998-080895
TI Minimising propagation delays caused by lead frame bonding finger length differences - using progressively elongated printed circuit conductors doubled-back beneath quad package to solder pad in central bonding region.
DC A85 L03 V04
IN HAMZEHDOOST, A; HUANG, C
PA (VLSI-N) VLSI TECHNOLOGY CORP
CYC 1
PI US 5742009 A 19980421 (199823)* 7p
ADT US 5742009 A US 1995-541213 19951012
PRAI US 1995-541213 19951012
AB US 5742009 A UPAB: 20000613

This novel printed **circuit board** layout, minimises signal delays caused by mismatch in the lengths of inner leads of a package lead frame. The printed **circuit board** is electrically-insulating and thermally-conducting. Bonding areas in rectangular configuration on the top surface, are disposed in the footprint of a quad flat pack. The conductive pattern formed on the printed **circuit board** includes U-shaped (108) metallised tracks. The first end of each track is joined to a bonding area, the second extends out from a central region of the board, near to a side edge of the quad flat pack. Each U-shape track is of varying length. Specific tracks near the inner leads at the package centre, are longer than others at the corners of the package lead frame. Preferably the board is ceramic, **FR4** board or epoxy-glass.

USE - To minimise clock delay caused by electrical conductor length mismatches and enhance device thermal dissipation into electrical conductors and **circuit board**.

ADVANTAGE - Length mismatch resulting from normally-convergent lead frame bonding fingers causes discrepancies in lead inductance, with corresponding propagation delays or clock skew. Electronic circuitry solutions are unsatisfactory. The method described both compensates for the delays, and assists thermal dissipation, by coupling thermal energy to the **circuit board** over a larger area. A 15%-30% decrease in thermal resistance is achieved.

Dwg.1/3

L10 ANSWER 28 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 1998-085677 [08] WPIX
DNN N1998-068060 DNC C1998-028921
TI Attaching integrated circuit component with solder bumps to substrate with bond pads - using anhydride containing flux such as methyl- hexa hydro-phthalic anhydride.
DC A21 A85 E13 L03 U11 V04
IN GAMOTA, D R; HERTSBERG, M; SCHEIFERS, S M; WILLE, S L
PA (MOTI) MOTOROLA INC

CYC 1
PI US 5704116 A 19980106 (199808)* 5p
ADT US 5704116 A US 1996-642708 19960503
PRAI US 1996-642708 19960503
AB US 5704116 A UPAB: 19980223
A method for attaching an integrated circuit component having solder bumps to a substrate having bond pads comprises: (a) dispensing onto the bond pads a solution containing an anhydride fluxing agent; (b) superposing the integrated circuit component onto the substrate so that each of the solder bump rests against one of the bond pads and is held by the fluxing agent; and (c) heating to bond the solder bumps to the bond pads and to vaporise the anhydride compound.

Also claimed is an encapsulant method for attaching an integrated circuit component to a substrate.

USE - The process is useful for mounting integrated circuits, e.g. on printed **circuit boards** (especially **FR4** board which is formed of a polymer layer laminated onto a ceramic or polymer/glass mesh core) using the flip-chip process or a ball grid array package onto bond pads, e.g. made of aluminium coated with a layer of chromium covered with copper.

ADVANTAGE - The anhydride can be vaporised during reflow of the solder bump interconnections, leaving no residue on the board which may interfere with under-filling of the component with a polymeric encapsulant. However, if any anhydride residue remains on the surface of the substrate, it can be readily solubilised into the encapsulant which includes an anhydride hardener similar to the anhydride in the fluxing agent. The substrate surface does not need to be cleaned prior to encapsulation and good encapsulation adhesion is achieved by incorporating any anhydride residue into the encapsulant. Anhydride fluxing agents provide more reliable connection than those containing acids, since anhydrides are more dielectric than acids and lead to better insulation and a lower chance of shorts between leads on the substrate.
Dwg.0/3

L10 ANSWER 29 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 1997-448937 [41] WPIX
DNN N1997-374096
TI Opto-electronic device packaging - has fibre-ferrule assembly with angle polishing to reduce back reflections.
DC P81 U12 V07
IN JIANG, C; MAK, E S; O'NEILL, S P; REYSEN, B H; ONEILL, S P; REYSEN, W H
PA (WHIT-N) WHITAKER CORP
CYC 30
PI WO 9732344 A1 19970904 (199741)* EN 11p
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: BR CA CN CZ FI HU JP KR MX NO PL RU SG
US 5857050 A 19990105 (199909)
ADT WO 9732344 A1 WO 1997-US2781 19970226; US 5857050 A Provisional US 1996-12463P 19960228, US 1997-808299 19970228
PRAI US 1996-12463P 19960228; US 1997-808299 19970228
AB WO 9732344 A UPAB: 19971013
Packaging is shown in cross section with the photodetector mounted on a substrate (103) with housing (101), spacer (102) and ferrule (105) for optical fibre (106). Elements (101,102,105) are preferably thermoplastic and the substrate is **FR4**, general **circuit board** material. Alignment in the z direction normal to the dielectric is fixed by the spacer with the ferrule stopped at the required z position.

If used in single mode fibre applications where the spot size is e.g. 40-60 microns in diameter, the fibre end-face may be 150-200 microns from the device. Curing is carried out by applying methylene chloride solvent

at the intersection of the spacer and housing, the substrate having been bonded to the spacer by epoxy.

USE - Packaging for optoelectronic devices, such as CATV.

Dwg.1/8

L10 ANSWER 30 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 1994-342736 [43] WPIX
DNN N1994-268913 DNC C1994-156125
TI Through-plating of printed **circuit boards** - by wetting the drilled board with a soln. of pyrrole, polymerising with acid oxidising soln., removing loose polymer and metallising.
DC A35 L03 M11 V04 X12
IN ROSCH, G; STUCKMANN, W; ROESCH, G
PA (GRUG) GRUNDIG EMV; (GRUG) GRUNDIG AG
CYC 42
PI DE 4314259 A1 19941103 (199443)* 4p
WO 9426082 A1 19941110 (199444) DE 20p
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL OA PT SE
W: AT AU BB BG BR CA CH CZ DE DK ES FI GB HU JP KP KR LK LU MG MN MW NL NO NZ PL PT RO RU SD SE SK UA US
AU 9466497 A 19941121 (199508)
EP 696410 A1 19960214 (199611) DE
R: AT BE CH DE FR GB IT LI NL
JP 08509578 W 19961008 (199705) 16p
DE 4314259 C2 19970410 (199719) 4p
EP 696410 B1 19970716 (199733) DE 7p
R: AT BE CH DE FR GB IT LI NL
DE 59403401 G 19970821 (199739)
US 5840363 A 19981124 (199903)
ADT DE 4314259 A1 DE 1993-4314259 19930430; WO 9426082 A1 WO 1994-EP1340 19940428; AU 9466497 A AU 1994-66497 19940428; EP 696410 A1 EP 1994-915137 19940428, WO 1994-EP1340 19940428; JP 08509578 W JP 1994-523886 19940428, WO 1994-EP1340 19940428; DE 4314259 C2 DE 1993-4314259 19930430; EP 696410 B1 EP 1994-915137 19940428, WO 1994-EP1340 19940428; DE 59403401 G DE 1994-503401 19940428, EP 1994-915137 19940428, WO 1994-EP1340 19940428; US 5840363 A Cont of US 1995-535122 19951027, US 1997-827594 19970328
FDT AU 9466497 A Based on WO 9426082; EP 696410 A1 Based on WO 9426082; JP 08509578 W Based on WO 9426082; EP 696410 B1 Based on WO 9426082; DE 59403401 G Based on EP 696410, Based on WO 9426082
PRAI DE 1993-4314259 19930430
AB DE 4314259 A UPAB: 19970522

A process is claimed for through-plating printed **circuit boards** by coating non-conducting parts of the board with a layer of electrically-conducting polymer (I) and then with metal. The polymer is applied directly to the base material of the board, and the process comprises: (a) wetting the whole surface of the board with a soln. of polymer-forming monomer, (b) polymerising the monomer by passing an acid, aq. soln. contg. oxidising agents over the board, and (c) removing loose polymer from the conducting parts of the board.

Pref., a horizontal technique is used, and in step (c) the polymer is removed from the conducting parts by spraying or flooding with the same acid soln. as used in (b). The through-plating holes can be produced by punching or drilling, and the metal layer consists of Cu, Ni, Au, Pd, Sn, Pb or Sn/Pb. The soln. for stage (a) contains monomer, organic solvent and water, pref. 1-20% pyrrole as monomer and 50-99% organic solvent and/or water, and the soln. for stage (b) contains 1-20% H_2SO_4, HCl or H_3PO_4, 1-20% alkali persulphate and/or 2-10% H_2O_2, the rest being water. The boards used are laminated with metal on both sides, and can be made of the base materials FR2, FR3 or CEM; if material **FR4** is used, the non-conducting parts are swollen with organic solvent before stage (a), pref. with the same solvent used in the soln. for stage (b).

USE - Used for through-plating of printed **circuit boards**.

ADVANTAGE - Enables high-quality metallisation in the holes without oxidative pretreatment, using cheaper base materials and with less environmental impact (no MnO2). The horizontal process (see below) ensures partic. rapid and reliable through-plating.

Dwg.0/0

L10 ANSWER 31 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 1994-100310 [12] WPIX
CR 1995-327677 [42]
DNC C1994-046202
TI Curable unsatd. polyester resin blend contg. brominated vinyl monomer - is economical and easily processed, useful as a high performance electrical insulation material in the electronic and microwave industries.
DC A23 A85 L03
IN BISHOP, S K; EVEN, T E; PERKEY, L M
PA (GLAS-N) GLASTEEL IND LAMINATES INC
CYC 1
PI US 5298314 A 19940329 (199412)* 9p
ADT US 5298314 A US 1991-756203 19910910
PRAI US 1991-756203 19910910
AB US 5298314 A UPAB: 19951102
A curable polyester resin blend comprising: (a) 30 - 80 wt.% first unsatd. polyester resin; and (b) 70 - 20 wt.% second unsatd. polyester resin, having degree of unsaturation 20 - 70%, less than that of (a), the polyester resins being derived from glycols and dibasic acids; (c) brominated vinyl monomer such that Br comprises 5 - 40 wt.% total resin blend; and (d) an effective amt. of a multi-tier, free-radical generating catalyst system for curing the blend, comprising at least 3 catalyst have half-lives approx. (i) 15 min. at 105 deg.C and 20 sec. at 145 deg.C (ii) 10 hrs. at 105 deg.C and 8 min. at 145 deg.C, and (iii) greater than 40 hrs. at 105 deg.C and 30 min. at 145 deg.C.

Z-axis expansion, 40 - 180 deg.C, is only 1.2 - 1.9%. Glass transition temp. is 140 - 180 deg.C and much smoother than that of **FR4** epoxy resin. It can withstand thermal stress of 260 deg.C (the temp. of molten solder), is less apt. to deform under other stresses, and is less brittle. Min. vol. resistivity is 1 x 108 megohms-cm, min. surface resistance 1 x 108 megohms, dissipation factor (1 MHz) 0.015, and dielectric constant (1 MHz) 3.2 - 3.8.

USE/ADVANTAGE - The resin blend is a high performance electrical insulation material useful in the electronic and microwave industries, e.g. as electronic **circuit boards** esp. in light weight avionics, low impedance microwave boards, EMI-RFI shielding, dielectric spacer, core restraining material. The blend is economical and easily processed and has high performance electrical, physical and mechanical properties allowing mfr. of highly reliable, very thin electrical components, allowing new designs in circuitry.

Dwg.0/0

Dwg.0/0

L10 ANSWER 32 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 1993-094256 [11] WPIX
CR 1993-151544 [18]; 1994-074129 [09]
DNN N1993-072115 DNC C1993-041727
TI High density contact socket for greater flexibility in **circuit board** design - has clip holding package against resilient contacts in insulating base.
DC A85 L03 U11 V04
IN CORBESERO, S R; DELPRETE, S D; SANTOS, D; DAMICO, R J
PA (AUGA-N) AUGAT INC

CYC 17
PI WO 9304512 A1 19930304 (199311)* EN 42p
RW: AT BE CH DE DK ES FR GB GR IT LU MC NL SE
W: CA JP
US 5215472 A 19930601 (199323) 17p
US 5221209 A 19930622 (199326) 20p
ADT WO 9304512 A1 WO 1992-US5615 19920702; US 5215472 A US 1991-748505 19910822; US 5221209 A CIP of US 1991-748505 19910822, US 1991-805366 19911211
PRAI US 1991-748505 19910822; US 1991-805366 19911211
AB WO 9304512 A UPAB: 19940418
A socket has resilient contacts (46) in holes (50) in an insulating part (42) and having a separable tip and base, and biasing to maintain alignment of connections between the contacts and a component installed in the socket. The biasing includes a U-shaped resilient clip with two beams parallel to the planar top surface of the component.

A socket cover applies pressure to hold the component in engagement with the contacts and there is a back-up fastener for connection to cover and/or socket. Holes are pref. lined with PTFE, nylon or **FR4** dielectric for crosstalk limitation, and there is insulating material between the fastener and a PCB on which the socket is mounted.

USE/ADVANTAGE - Partic. for mounting a leadless component package. Permits greater flexibility in **circuit board** architecture.
Dwg.2A/12
Dwg.2A/12

L10 ANSWER 33 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 1991-066435 [10] WPIX
DNC C1991-028110
TI Direct metallisation of non-conductive polymer substrate - by electroplating onto reduced or thermally decomposed metal cpd. layer.
DC A35 A85 L03 M11
IN MAJENTNY, K; MIDDEKE, H J
PA (SCHD) SCHERING AG
CYC 1
PI DE 3928434 A 19910228 (199110)*
ADT DE 3928434 A DE 1989-3928434 19890824
PRAI DE 1989-3928434 19890824
AB DE 3928434 A UPAB: 19930928
Direct metallisation of a non-conductive substrate, esp. for printed circuit mfr., involves (a) pre-cleaning, opt. etching or swelling of the surface to be metallised; (b) covering the . surface with a metal cpd., pref. a water-insol. metal cpd. (esp. resinate) with a positive redox potential or a metal complex; (c) reducing or thermally decomposing the metal cpd. to the metal; and (d) electroplating, e.g. with copper or nickel.

USE/ADVANTAGE - Used esp. for metallising **circuit board** materials e.g. FR3 and **FR4**, comprising polymers e.g. polyimide, epoxy or phenolic resins, ceramic surfaces, glass or composite materials. Electroless plating is eliminated, thus simplifying the process and increasing finished circuit quality.
0/0

L10 ANSWER 34 OF 36 WPIX (C) 2003 THOMSON DERWENT
AN 1991-049249 [07] WPIX
DNN N1991-037943 DNC C1991-021186
TI Seed process for low dielectric materials, for printed **circuit board** - by immersing fluoro-polymer substrate in solvent of noble metal salt, and alkaline reducing agent etc..
DC A14 A35 L03 M13 V04

PA (ANON) ANONYMOUS
CYC 1
PI RD 321054 A 19910110 (199107)*
PRAI RD 1990-321054 19901220
AB RD 321054 A UPAB: 19930928
One of first steps in metallisation of printed **circuit boards** (PCB) is deposition of electroless copper. While subsequent circuitisation processes may vary, electroless copper deposition is common to most and comprises application of seed layer (pref. noble metal catalyst) then immersion in electroless copper bath. Most seed/electroless processes have been designed for applications with **FR4** epoxy substrates. Using dielectric materials other than **FR4** is often dictated by increased PCB performance requirements. Fluoropolymers e.g. PTFE or PFA and filled composites of these materials, are now used as PCB materials due to their low dielectric constants and pref. thermal expansion properties. Metallisation of these materials is difficult producing numerous voids and poorly adherent metal, attributable to poor wetting of polymer surface. Described herein is seeding method which enables electroless copper metallisation of many perfluoronated substrates under ambient process conditions, i.e., does not require rigorous oxygen exclusion. Fluoropolymer substrate is immersed in non-aq. solvent (e.g., NMP, DMF, DMSO) contg. noble metal salt or complex (e.g., palladium acetylacetonate or palladium (II) chloride). Metal complex or salt is absorbed onto or absorbed into dielectric surface. This is followed by immersion of substrate into alkaline reducing agent (e.g., sodium borohydrate) so noble metal complex is reduced to its catalytically active, zero valent state. Metal complexes or salts are insol. in alkaline reducing agent so little or no catalyst is lost from dielectric substrate surface. Following brief aq. rinse substrate may be immersed in conventional electroless copper plating bath.

L10 ANSWER 35 OF 36 JAPIO COPYRIGHT 2003 JPO
AN 2002-043006 JAPIO
TI SOCKET CONNECTOR
IN STEFFANIE CLEVELAND
PA BERG TECHNOL INC
PI JP 2002043006 A 20020208 Heisei
AI JP 2001-171183 (JP2001171183 Heisei) 20010606
PRAI US 2000-593561 20000614
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To provide a zero-insert force connector, having a base with a coefficient of thermal expansion similar to or the same as that of a printed **circuit board**.
SOLUTION: This invention discloses a socket for connecting an electronic component to a **circuit board**. At least a part of the base of the socket is made of an epoxy resin material filled with glass, such as **FR4**, which is the same as that of the **circuit board**. The socket has a cover grounded on the base, a contact for engaging a male contact with an electronic component, and an actuator for moving the cover with respect to the base. The socket can be surface-mounted on the **circuit board** by a fusible member such as a solder ball.
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L10 ANSWER 36 OF 36 JAPIO COPYRIGHT 2003 JPO
AN 1999-251145 JAPIO
TI SUSPENDED PRINTED INDUCTOR AND LC-FORMAT FILTER CONSTITUTED OF THE SAME
IN ALEXANDER MOSTOV
PA BUTTERFLY VLSI LTD
PI JP 11251145 A 19990917 Heisei
AI JP 1998-295194 (JP10295194 Heisei) 19981016

PRAI US 1998-4777 19980109
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To cause a suspended printed inductor to have a high quality coefficient and reproducibility with the inductance value improved, by causing the suspended printed inductor to include an electrically conductive trace printed on a board and a region below the trace lacking a ground plate of the board.
SOLUTION: A suspended printed inductor 10 has a rectangular spiral trace 32 on the upper side of a printed **circuit board**(PCB) 30. The PCB 30 is made of a board material having appropriate physical and electrical characteristics, for example, a standard printed **circuit board** material such as **FR4**. The inductor trace 32 is printed on the one side, that is, the upper side of the PCB 30, and the other side or lower side of the PCB 30 does not have a ground plane below the inductor trace 32. Two metal covers 40 and 42 of the suspended printed inductor are mounted on the respective sides of the PCB 30 and are electrically connected to a ground potential. The metal covers effectively shield electric circuit elements.

L22 ANSWER 1 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2002-680764 [73] WPIX
DNN N2002-537264 DNC C2002-192081
TI Integral dielectric heat spreader for transferring heat from semiconductor devices comprises thermally conductive electrically insulating material having first central area and at least one conductive pad.
DC L03 V04
IN HUTCHISON, B R; SCHWIEBERT, M; THOMPSON, R J
PA (AGIL-N) AGILENT TECHNOLOGIES INC
CYC 1
PI US 6414847 B1 20020702 (200273)* 5p
ADT US 6414847 B1 US 2001-829453 20010409
PRAI US 2001-829453 20010409
AB US 6414847 B UPAB: 20021113
NOVELTY - Integral dielectric heat spreader comprises a thermally conductive electrically insulating material having a first central area for mounting the semiconductor device on a first surface of the heat spreader, and at least one conductive pad on the first surface for accepting **electrical connections** from the device to the conductive pad and from the conductive pad to the secondary surface.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a method of mounting a semiconductor device (100), which comprises mounting the device to an integral dielectric heat spreader (110) containing at least one conductive feature, mounting the heat spreader on a secondary surface containing conducting layers, and connecting the device to at least one conductive feature on the secondary surface via at least one conductive feature on the heat spreader.

USE - The integral dielectric heat spreader is used for transferring heat from semiconductor devices. It is used to mount high power semiconductor devices to a printed **circuit board** (120).

ADVANTAGE - The dielectric heat spreader provides thermal transfer between the semiconductor device and a printed **circuit board**. Thermal performance of the printed **circuit board** is improved by providing thermal vias (130) which provide additional heat transfer from the dielectric heat spreader.

DESCRIPTION OF DRAWING(S) - The figures show a cross section of a dielectric head speaker.

semiconductor device 100
heat spreader 110
printed **circuit board** 120
thermal vias 130
Dwg.1,2/3

L22 ANSWER 2 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2002-320393 [36] WPIX
DNN N2002-250941
TI Printed **circuit board** has auxiliary wiring pattern formed on specified area of semiconductor chip, which is **electrically connected** to wiring pattern of substrate.
DC U11 U14 V04 X15
PA (MATU) MATSUSHITA DENKI SANGYO KK
CYC 1
PI JP 2001332866 A 20011130 (200236)* 15p
ADT JP 2001332866 A JP 2000-152621 20000524
PRAI JP 2000-152621 20000524
AB JP2001332866 A UPAB: 20020610
NOVELTY - An auxiliary wiring pattern (108) formed on a specified area of a semiconductor chip (105) is **electrically connected**

to wiring patterns (102, 103) of substrate of the **circuit board**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for printed **circuit board** manufacturing method.

USE - Printed **circuit board** (PCB) with built-in active and **passive components** such as semiconductor chip and capacitor.

ADVANTAGE - High density wiring formation is realized by enhancing the rate of wiring held.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the PCB.

Substrate wiring pattern 102, 103
Semiconductor chip 105
Auxiliary wiring pattern 108

Dwg.1/12

L22 ANSWER 3 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2002-268553 [31] WPIX
DNN N2002-209010
TI Radio communications module for short-ranges and wireless local area networks includes multi-layer printed **circuit board**, integrated antenna and **passive components**.
DC V04 W01 W02
IN GONG, S; NILSSON, J
PA (BLUE-N) BLUETRONICS AB
CYC 94
PI WO 2001095679 A1 20011213 (200231)* EN 10p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2001056895 A 20011217 (200231)
SE 2000001943 A 20011208 (200231)
ADT WO 2001095679 A1 WO 2001-SE949 20010503; AU 2001056895 A AU 2001-56895 20010503; SE 2000001943 A SE 2000-1943 20000607
FDT AU 2001056895 A Based on WO 200195679
PRAI SE 2000-1943 20000607
AB WO 200195679 A UPAB: 20020516
NOVELTY - A radio communications module includes a carrier in the form of a laminated multi-layer printed **circuit board** (PCB) card (1). A first side (11) of the card has an integrated antenna (10).

DETAILED DESCRIPTION - A radio frequency (RF) chip (13) is surface-mounted on the other side (12) of the card that also has terminals (16, 17) in the form of Ball Grid Array (BGA) balls. **Passive components** (14, 15), such as filters, inductors and capacitors, are integrated in the PCB-card and connected to vias.

USE - The radio communications module is used for short-ranges and wireless local area networks.

ADVANTAGE - The module can be made very small. A high radio quality is achieved owing to the absence of parasitic capacitances and inductances in **electrical connectors**. The module has a high sensitivity since components are integrated in the structure. The cost of manufacture is low.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of a radio communications module.

Printed **circuit board** (PCB) card 1
Antenna 10
First side 11
Second side 12

Radio frequency (RF) chip 13
Integrated **passive components** 14, 15
Ball grid array (BGA) terminals 16, 17
Dwg.1/4

L22 ANSWER 4 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2002-268022 [31] WPIX
CR 2002-026100 [70]; 2002-061955 [68]; 2002-179320 [67]; 2002-268023 [67]; 2002-268026 [67]
DNN N2002-208489
TI **Connecting** element for **electrical** components has hollow metal core allowing component mounting in or outside on high density interconnect film.
DC U11 V04 V07
IN SCHMIDT, W
PA (DYCO-N) DYCONEX PATENTE AG
CYC 95
PI WO 2001076330 A1 20011011 (200231)* EN 31p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2001039090 A 20011015 (200231)
ADT WO 2001076330 A1 WO 2001-CH193 20010329; AU 2001039090 A AU 2001-39090 20010329
FDT AU 2001039090 A Based on WO 200176330
PRAI US 2000-193370P 20000331
AB WO 200176330 A UPAB: 20020516
NOVELTY - Connection element is metal (1, 3) with optional central cavity (101) so components mounted outside on high density interconnect (HDI) film (5, 5') can link to components on other side through central core or around outside. Fibre optic connections (105, 105') can be made through core providing high accuracy of join. Additional core heat pipes may be added.
DETAILED DESCRIPTION - An independent claim is also included for a method of producing the connecting element.
USE - Used for **connecting electrical** components and optical fibres.
ADVANTAGE - Provides additional functions beyond that of a **circuit board** including providing impedance values, EM shielding layers, embedded **passive components**, optical interconnects and ease of reuse or recycling.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross section of the connecting element.
Metal core 1, 3
HDI film 5, 5'
Central cavity 101
Thermal connection 103, 103'
Optical fibre 105, 105'
Dwg.9a/11

L22 ANSWER 5 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2002-212843 [27] WPIX
DNN N2002-162807
TI **Electrical connector** for testing electronic component, has contact probe pin with movable plungers with opposing magnets provided inside conducting cylinder.
DC S01
PA (KITA-N) KITA SEISAKUSHO KK; (NISS-N) NISSHO IWAI PLASTIC HANBAI KK

CYC 1
PI JP 2002042945 A 20020208 (200227)* 7p
ADT JP 2002042945 A JP 2000-230630 20000731
PRAI JP 2000-230630 20000731
AB JP2002042945 A UPAB: 20020429
NOVELTY - A contact probe pin (1) has hollow conducting cylinder (3) with movable plungers (5,17) whose contact portions (4,16) protrude from the openings (2,15) at the ends of the cylinders. Magnets (7,10) are fixed to the plunger surfaces such that the like poles of the magnets oppose mutually. The contact portion is connected to a semiconductor device terminal (14).

USE - For testing electrical property of electronic components such as **passive components**, functional components and conversion components mounted in printed wiring board and display devices.

ADVANTAGE - Heat and corrosion resistance is high, hence stable electrical property measurement is enabled in both low and high frequency regions of the electronic component.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the contact probe pin.

Contact probe pin 1
Openings 2,15
Hollow conducting cylinder 3
Contact portions 4,16
Movable plungers 5,17
Magnets 7,10
Semiconductor device terminal 14
Dwg.2/3

L22 ANSWER 6 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2001-513617 [56] WPIX
CR 2002-120890 [16]
DNN N2001-380416
TI **Electrical connection** method in integrated circuit packaging, involves **connecting electrical connection** points of **passive components** with termination pads of semiconductor device and cavity of substrate.
DC U11
IN FAROOQ, M S; KNICKERBOCKER, J U; REDDY, S S
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 2001010398 A1 20010802 (200156)* 9p
US 6489686 B2 20021203 (200301)
ADT US 2001010398 A1 Div ex US 1999-469157 19991221, US 2001-812091 20010319; US 6489686 B2 Div ex US 1999-469157 19991221, US 2001-812091 20010319
FDT US 2001010398 A1 Div ex US 6228682; US 6489686 B2 Div ex US 6228682
PRAI US 1999-469157 19991221; US 2001-812091 20010319
AB US2001010398 A UPAB: 20030101
NOVELTY - Electrical termination pads (42) are provided on cavities (30) in substrate (50). Passive electrical components (10) with connection points (40) are placed in the cavities such that the location of a connection point corresponds with the termination pad. A semiconductor device is placed over the **passive component** such that its termination pad location corresponds with the other connection point of the **passive component**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for structure for **electrically connecting** discrete components between semiconductor substrate and semiconductor device.

USE - For **electrical connection** between passive electronic component such as resistors, capacitors, inductors, filters, semiconductor substrate and device in integrated circuit (IC) packaging.

ADVANTAGE - Minimizes the lead lengths between **passive**

components, semiconductor substrate and semiconductor device.
DESCRIPTION OF DRAWING(S) - The figure shows the semiconductor structure attached to semiconductor **circuit board**.
Passive electrical components 10
Cavities 30
Connection points 40
Electrical termination pads 42
Substrate 50
Dwg.2/4

L22 ANSWER 7 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2001-455559 [49] WPIX
DNN N2001-337629
TI Module substrate for electronic components such as semiconductor integrated circuit, has **motherboard** connected to substrate using solder provided to electrode which is made to project ahead from end face of substrate.
DC V04 X24
PA (MURA) MURATA MFG CO LTD
CYC 1
PI JP 2001160666 A 20010612 (200149)* 13p
ADT JP 2001160666 A JP 1999-341229 19991130
PRAI JP 1999-341229 19991130
AB JP2001160666 A UPAB: 20010831
NOVELTY - Electrode (15) is provided to the end face (11C) of substrate (11) and is connected to electronic component mounted on substrate. The **motherboard** provided to the back side is **electrically connected** to substrate using solder (17) which is provided to electrode and is made to project ahead from the end face of substrate.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for module substrate manufacturing method.
USE - Module substrate for electronic components such as semiconductor integrated circuit (IC), active and **passive components** which are used in electronic devices.
ADVANTAGE - As the solder is made to project from end face of substrate, several solders are mounted in end face electrode and hence the back side of a substrate is made to suspend, with a row of solder joined at end face electrode side. End face electrode is reliably connected to **motherboard**, even when a curvature is produced in substrate.
DESCRIPTION OF DRAWING(S) - The figure shows the enlarged perspective diagram of end-face through hole. (Drawing includes non-English language text).
Substrate 11
End face of substrate 11C
Electrode 15
Solder 17
Dwg.2/19

L22 ANSWER 8 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2001-446763 [48] WPIX
DNN N2001-330408
TI Electrical property measurement for portable telephone, involves deforming retainer holding measured object by pressing, such that terminals of measured object and measurement machine, are **connected electrically**.
DC S01
PA (HITK) HITACHI METALS LTD
CYC 1
PI JP 2001153907 A 20010608 (200148)* 4p
ADT JP 2001153907 A JP 1999-333367 19991124
PRAI JP 1999-333367 19991124

AB JP2001153907 A UPAB: 20010829
NOVELTY - A retainer (5) holding the measured object (1), is pressed. The retainer deforms on pressing such that terminals of measured object and measurement machine (2) are **connected electrically**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the workpiece holder.
USE - For inspecting electrical property of **passive components** used in RF circuit section of portable telephone.
ADVANTAGE - Enables measuring electrical property correctly without connecting the external electrode terminal of the workpiece, to terminal of measuring jig. The inspection time is reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the workpiece holder.
Measured object 1
Measurement machine 2
Retainer 5
Dwg.1/3

L22 ANSWER 9 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2001-100958 [11] WPIX
DNN N2001-220960 DNC C2001-095543
TI Surface mounted composite RC device including capacitor made of ceramic layers.
DC L03 V01
IN BLAIR, A; HEISTAND, R H; MOORE, C A; RITTER, A P; STRAWHORNE, M; ANDREW, B; RITTER, A
PA (AVXA-N) AVX CORP; (BLAI-I) BLAIR A; (HEIS-I) HEISTAND R H; (MOOR-I) MOORE C A; (RITT-I) RITTER A P; (STRA-I) STRAWHORNE M
CYC 32
PI NO 2000003015 A 20001219 (200111)*
JP 2001044076 A 20010216 (200114) 14p
CZ 2000002277 A3 20010214 (200119)
CN 1279533 A 20010110 (200128)
EP 1061535 A2 20001220 (200133)B EN 21p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
KR 2001021003 A 20010315 (200159)
US 2002011905 A1 20020131 (200210)
US 2002041219 A1 20020411 (200227)
US 2002044029 A1 20020418 (200228)
TW 452808 A 20010901 (200240)
ADT NO 2000003015 A NO 2000-3015 20000613; JP 2001044076 A JP 2000-182939 20000619; CZ 2000002277 A3 CZ 2000-2277 20000616; CN 1279533 A CN 2000-118363 20000616; EP 1061535 A2 EP 2000-304693 20000602; KR 2001021003 A KR 2000-33440 20000617; US 2002011905 A1 Div ex US 1999-335991 19990618, US 2001-871252 20010531; US 2002041219 A1 Div ex US 1999-335991 19990618, US 2001-871251 20010531; US 2002044029 A1 Div ex US 1999-335991 19990618, US 2001-871237 20010531; TW 452808 A TW 2000-111930 20000617
PRAI US 1999-335991 19990618; US 2001-871252 20010531; US 2001-871251 20010531; US 2001-871237 20010531
AB EP 1061535 A UPAB: 20010615 ABEQ treated as Basic
NOVELTY - The device includes a device body having a stack of 1st and 2nd ceramic layers. Each of the ceramic layers has a corresponding electrode plate arranged such as to form two plates of a capacitor. The 1st or 2nd electrode plates are partially formed of a cofireable resistor material. The device body has a pair of terminations electrically connected to the 1st electrode plates and at least one termination electrically connected to the 2nd electrode plate to provide a predetermined electrical function.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(a) an array device having a given number of RC circuits in a single package a miniature surface mounted device comprising a number of pressed

and sintered ceramic-electrode layers and a device body with an inner metal oxide termination layer and an outer solderable metal termination layer the fabrication of a composite RC device; and

(b) further a composite RC device.

USE - Multilayer ceramic structure electronic components.

ADVANTAGE - Improved termination structure.

DESCRIPTION OF DRAWING(S) - The diagram shows a perspective of a surface mounted RC filter array in position on a **circuit board**.

RC array 10

Circuit board 12

Main body 14

Terminals 16a-d,18a-d,20,22

Dwg.1/20

AB NO 200003015 A UPAB: 20010620

NOVELTY - The device includes a device body having a stack of 1st and 2nd ceramic layers. Each of the ceramic layers has a corresponding electrode plate arranged such as to form two plates of a capacitor. The 1st or 2nd electrode plates are partially formed of a cofireable resistor material. The device body has a pair of terminations electrically connected to the 1st electrode plates and at least one termination electrically connected to the 2nd electrode plate to provide a predetermined electrical function.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(a) an array device having a given number of RC circuits in a single package a miniature surface mounted device comprising a number of pressed and sintered ceramic-electrode layers and a device body with an inner metal oxide termination layer and an outer solderable metal termination layer the fabrication of a composite RC device; and

(b) further a composite RC device.

USE - Multilayer ceramic structure electronic components.

ADVANTAGE - Improved termination structure.

DESCRIPTION OF DRAWING(S) - The diagram shows a perspective of a surface mounted RC filter array in position on a **circuit board**.

RC array 10

Circuit board 12

Main body 14

Terminals 16a-d,18a-d,20,22

Dwg.1/20

L22 ANSWER 10 OF 28 WPIX (C) 2003 THOMSON DERWENT

AN 2000-639646 [62] WPIX

DNN N2000-474352

TI Passive electronic component, especially capacitor - has insulating layer which can be removed to place component in activated state.

DC S01 U11 U12 V01 V02 V04 X12

IN BUCHNER, R

PA (SIEI) SIEMENS AG

CYC 1

PI DE 19918625 A1 20001102 (200062)* 4p

ADT DE 19918625 A1 DE 1999-19918625 19990423

PRAI DE 1999-19918625 19990423

AB DE 19918625 A UPAB: 20001130

An activation device (7) causes the **passive component** to irreversibly change from a deactivated state to an activated state. The activation device is operated externally by applying an external force. A first contact group is **electrically connected** to the component body. A second contact group is connected to external connection points.

The activation device is arranged between the first and second

contact groups. The activation device may be an insulating layer or film, with an actuating part for removing the insulating layer.

USE - For in-circuit testing of electronic components on common substrate especially integrated circuit.

ADVANTAGE - Simplifies testing and makes it more reliable.

Dwg.2/3

L22 ANSWER 11 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2000-586897 [55] WPIX
DNN N2000-434359 DNC C2000-174883
TI Metal oxide ceramic material is rendered electrically conductive by the incorporation of silver into the material, e.g. for bipolar plates for solid oxide fuel cells.
DC L03 U11 V04 W02 X12 X16
IN JAFFREY, D
PA (CERA-N) CERAMIC FUEL CELLS LTD
CYC 91
PI WO 2000040520 A1 20000713 (200055)* EN 21p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2000022689 A 20000724 (200055)
EP 1147070 A1 20011024 (200171) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
JP 2002534769 W 20021015 (200282) 25p
ADT WO 2000040520 A1 WO 1999-AU1140 19991223; AU 2000022689 A AU 2000-22689 19991223; EP 1147070 A1 EP 1999-966780 19991223, WO 1999-AU1140 19991223; JP 2002534769 W WO 1999-AU1140 19991223, JP 2000-592235 19991223
FDT AU 2000022689 A Based on WO 200040520; EP 1147070 A1 Based on WO 200040520; JP 2002534769 W Based on WO 200040520
PRAI AU 1998-7988 19981231
AB WO 200040520 A UPAB: 20001102
NOVELTY - Metal oxide ceramic material is rendered electrically conductive through its thickness by the incorporation of silver into the material.

DETAILED DESCRIPTION - INDEPENDENT CLAIMs are also included for

(1) a component formed of steel having a surface layer of alumina, chromia, or alumina-rich or chromia-rich ceramic, this layer having been rendered electrically conductive through its thickness by the incorporation of silver into the layer,

(2) a method of providing electrical conductivity through metal oxide ceramic material, and

(3) a method of forming a steel component with a heat-resistant and electrically conductive surface layer.

USE - Creation of electrical conductivity in a normally **non-conductive ceramic** material, the layer of metal oxide ceramic can be adhered to a metal plate, for bipolar plates, current collector straps and heat exchangers for solid oxide fuel cells. For printed **circuit boards**, microelectronics, semiconductors, wave guides and sensors.

ADVANTAGE - The invention can provide, with alumina, a material which is still an excellent refractory material and inert in nearly all environments, but which is electrically conductive at least in selected positions. The effect is durable over long periods of time and over the full temperature range required for solid oxide fuel cell operation.

Dwg.0/3

L22 ANSWER 12 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2000-557784 [51] WPIX

DNN N2000-412753 DNC C2000-166014
TI Surface-mount device package, e.g. ball grid array device for integrated circuit chip includes pad, terminal, and electrically resistive volume.
DC L03 U11
IN DUNN, G J; GAMOTA, D R; LACH, L E
PA (MOTI) MOTOROLA INC
CYC 1
PI US 6108212 A 20000822 (200051)* 12p
ADT US 6108212 A US 1998-92637 19980605
PRAI US 1998-92637 19980605
AB US 6108212 A UPAB: 20001016
NOVELTY - A surface-mount device package comprises a pad, terminal, and an electrically resistive volume to form a **passive component** associated with at least one external or internal device interconnection.

DETAILED DESCRIPTION - The package (60) comprises a pad (27) on a face of the device, a solder bump (28) bonded to the pad, a terminal (34) on the face and surrounding the pad to be spaced apart from the pad, and an electrically-resistive volume (36) intervening the pad and terminal. The pad is a component an internal or external **electrical connections** (64, 66) of the device. It is coupled to the terminal through the resistive volume to define an integral resistor (32).

USE - The surface-mount device package, e.g. ball grid array (BGA) is used in an integrated circuit chip.

ADVANTAGE - The integral resistor eliminates or at least reduces electrical resonance and reflections that may degrade the signal integrity. The electrical system reliability associated with a printed wiring board, an IC, and a BGA package may increase through the use of the integral resistor. Increases the maximum potential circuit density of printed **circuit boards** by replacing discrete **passive components** with integral **passive components** that use less **circuit board** space rather than the discrete components.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of the device.

die 12
interposer 14
pad 27
solder bump 28
integral resistor 32
terminal 34
conductive plate 44
dielectric region 46
faces 52,54
surface-mount device 60
internal and external **electrical connections** 64,66
Dwg.1/10

L22 ANSWER 13 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 2000-107392 [10] WPIX
DNN N2000-082508
TI Electronic flexible type **circuit board** especially for power semiconductors, sensors and **passive components** - uses plastics layer as basic carrier with at least one recess extending through it.
DC U11 V04
IN ROEDIG, H; ZELLNER, M
PA (SIEI) SIEMENS AG
CYC 1
PI DE 19830540 A1 20000113 (200010)* 8p

ADT DE 19830540 A1 DE 1998-19830540 19980708
PRAI DE 1998-19830540 19980708
AB DE 19830540 A UPAB: 20000228
An electronic circuit flexible board includes a basic carrier or support for the electronic components, which have at least one contact (6), and a network of conductor paths (9). The basic carrier is a plastics layer (1) having at least one recess running through it, the recess being in alignment with the corresponding contact (6) of the electronic component (2,3) fixed on the plastics layer (4).

A metallisation layer (8) is provided on the plastics layer (4) and forms the network of conductors which **electrically joins** the contact (6) through the corresponding recess (7). The plastics layer is more specifically a plastics film or foil.

ADVANTAGE - Space-savings arrangement of electric components having closely positioned contacts.

Dwg.1/5

L22 ANSWER 14 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1999-504522 [42] WPIX
DNN N1999-377330
TI High frequency chip module - is **electrically connected** to **motherboard** by bump formed on electrode of each mounted chip component.
DC U11
PA (TAMA-N) TAMA DENKI. KOGYO KK
CYC 1
PI JP 11220089 A 19990810 (199942)* 3p
ADT JP 11220089 A JP 1998-32126 19980129
PRAI JP 1998-32126 19980129
AB JP 11220089 A UPAB: 19991207
NOVELTY - The circuit module consists of semiconductor device and **passive component** part (5). The chip module is **electrically connected** to the **motherboard** by a bump formed on the electrode of each mounted chip component.

USE - High frequency chip module.

ADVANTAGE - Since resistor, capacitor and inductor are formed as **passive component**, space saving is attained. Therefore high frequency characteristic can be obtained. DESCRIPTION OF DRAWING(S) - The figure shows the mounting condition of the chip module. (5) **Passive component** part.

Dwg.2/5

L22 ANSWER 15 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1999-174076 [15] WPIX
DNN N1999-128095
TI Overcurrent protection circuit for speakers - has **resistive conductive** materials stuck to dampers holding voice coil.
DC V06
PA (TRIR) KENWOOD CORP
CYC 1
PI JP 11027785 A 19990129 (199915)* 4p
ADT JP 11027785 A JP 1997-195128 19970704
PRAI JP 1997-195128 19970704
AB JP 11027785 A UPAB: 19990416
NOVELTY - The circuit has resistive material (4a) and conductive materials (5a) stuck to dampers (4,5) that holds a voice coil. An overcurrent protection switch is also provided in the circuit.

USE - For speakers.

ADVANTAGE - Achieves space saving since resistance is not mounted on the printed **circuit board**. Since there is no closed loop coil that generates counter emf, degradation of the quality is

reduced. DESCRIPTION OF DRAWING(S) - The figure shows the plan of the protective circuit. (4a) Resistive material; (4,5) Dampers; (5a) Conductive materials.
Dwg.2/8

L22 ANSWER 16 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1998-390371 [34] WPIX
DNN N1998-304565 DNC C1998-118118
TI Production of housing for packaging microwave component, for PCB - comprises fixing component and frame to substrate, wiring **electrical connections**, depositing **electrically** insulating material, grinding, and forming microwave circuit.
DC A85 L03 U11 U23 U24 V01
IN CACHIER, G; GRANCHER, A; VAL, C
PA (CSFC) THOMSON CSF SA
CYC 1
PI FR 2758417 A1 19980717 (199834)* 22p
ADT FR 2758417 A1 FR 1997-415 19970116
PRAI FR 1997-415 19970116
AB FR 2758417 A UPAB: 19980826
Production of a microwave component package housing comprises: (a) fixing the component (23) and a surrounding frame (22) on a substrate (21); (b) wiring **electrical connections** (27) between the component and the upper surface of the frame; (c) depositing a first electrically insulating material (25) on the component and the substrate and then grinding the layer until it is flush with the connections on the upper surface; (d) forming a microwave circuit, including conductive lines (33) that extend radially on the upper surface and have first ends in electrical contact with the connections and second ends forming housing input, output connection zones, the circuit having an input, output impedance of predetermined value, preferably 50 ohms.

Also claimed is a package housing produced by the above process, in which the first insulating material is preferably epoxy resin.

USE - Used to make a packaged semiconductor chip, for mounting on a **circuit board**, including a discrete or integrated active component (amplifier, mixer, switch, oscillator, etc.) or a **passive component** (capacitor, resistor, etc.) operating in the millimetre wavelength microwave range.

ADVANTAGE - The packaged component can be surface mounted on a printed **circuit board** without strict mounting tolerances, is easily subjected to electrical testing, is simple to produce at reduced cost and has microwave earth continuity and minimal parasitic elements (e.g. series inductance or parallel capacitance) at its pads.
Dwg.4/6

L22 ANSWER 17 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1998-231099 [20] WPIX
DNN N1998-182951
TI **Passive component** with 2 connections with plugin securing component to PCB - has pins of each plug different in length and width enabling manual installation of component in correct position in simplified manner, pins are positioned so that four pins are not situated in flat plane.
DC V01 V04
IN DIJKSTRA, R
PA (PHIG) KONINK PHILIPS ELECTRONICS NV; (BCCO-N) BC COMPONENTS HOLDINGS BV; (PHIG) PHILIPS ELECTRONICS NV; (PHIG) PHILIPS NORDEN AB
CYC 19
PI WO 9814039 A1 19980402 (199820)* EN 12p
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

W: JP
EP 868838 A1 19981007 (199844) EN
R: DE FR GB NL
US 5921820 A 19990713 (199934)
JP 2000501572 W 20000208 (200018) 11p
ADT WO 9814039 A1 WO 1997-IB888 19970717; EP 868838 A1 EP 1997-929456 19970717, WO 1997-IB888 19970717; US 5921820 A US 1997-935594 19970923; JP 2000501572 W WO 1997-IB888 19970717, JP 1998-515446 19970717
FDT EP 868838 A1 Based on WO 9814039; JP 2000501572 W Based on WO 9814039
PRAI EP 1996-202668 19960924
AB WO 9814039 A UPAB: 19980520
The **passive component** (1) has two **electric connections** with plug in parts for securing and **electrically connecting** component to printed **circuit board**. Both plug in parts have two pins and are positioned so that the four pins (5, 5', 6 and 6') are not situated in a flat plane.

The pins of each plug in part are different in length and width enabling manual installation of component in correct position in simplified manner. The component is in the form of an electrolytic capacitor with curved pins which are resilient relative to each other.

USE - For securing and **electrically connecting** component to printed **circuit board**.

ADVANTAGE - Aims at providing **passive component** which can be secured in reliable manner without resoldering using wave soldering treatment to give electric contact.

Dwg.1A/2

L22 ANSWER 18 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1997-251751 [23] WPIX
DNN N1997-208178
TI Flat antenna for antenna apparatus used in reception of electromagnetic wave from artificial satellite - has ground electrode, filter pattern and circuit pattern, which are arranged in layers in ceramic dielectric, that are **electrically connected** to emission electrode.
DC W02 W06
PA (MATU) MATSUSHITA DENKI SANGYO KK
CYC 1
PI JP 09083239 A 19970328 (199723)* 9p
ADT JP 09083239 A JP 1995-230900 19950908
PRAI JP 1995-230900 19950908
AB JP 09083239 A UPAB: 19970606
The antenna has an emission electrode (1), a ground electrode (2), a filter pattern (3) and a circuit pattern (5) which are arranged in layers in a ceramic dielectric (4). The ground electrode, filter pattern and circuit pattern are **electrically connected** to the emission electrode.

USE/ADVANTAGE - For communication system e.g. global positioning system. Reduces size of antenna and can be cost effectively manufactured by not using **passive component** e.g. printed **circuit board**, filter, capacitor, inductor, resistor. Enables mass production through highly efficient and highly reliable manufacture due to layered composition. Improves operativity, and reduces cost and production mandays by canceling use of feeder path e.g. pin. Obtains high gain by reducing signal transmission loss, thus improving antenna quality. Obtains reliable filter characteristic due to function of filter pattern.

Dwg.1/21

L22 ANSWER 19 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1996-430809 [43] WPIX

DNN N1996-363174
TI Hybrid integrated circuit - has holder that is joined to metal substrate whose sides are bent to form U-shaped metal substrate.
DC U14 V04
PA (SAOL) SANYO ELECTRIC CO LTD
CYC 1
PI JP 08213733 A 19960820 (199643)* 6p
ADT JP 08213733 A JP 1995-14295 19950131
PRAI JP 1995-14295 19950131
AB JP 08213733 A UPAB: 19961025
The circuit (1) has an insulated layer provided in a rectangular metal substrate (3). Electrical conductors such as wirings, lands, pads, and lead terminals are provided on the insulated layer. A **passive component** is **connected electrically** to an active component.

A lead terminal is **electrically connected** to one side of the metal substrate. An external lead terminal is **electrically connected** to the other side of the magnetic substrate opposite the lead terminal. The sides of the metal substrate are bent to form a U-shaped metal substrate that is joined to a holder (40).

ADVANTAGE - Simplifies design of printed **circuit board**; suppresses generation of cracks on metal substrate by providing holder; prevents external noise from influencing circuit operation; develops structure enabling component to be positioned on printed **circuit board** that is coupled with installation area.
Dwg.1/7

L22 ANSWER 20 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1996-430669 [43] WPIX
DNN N1996-363034
TI Hybrid-integrated-circuit appts. - has metal substrate set up in way that it passes into regular-interval inner side from opposite side edge, in which installation surface is bent into U-shape.
DC U14
PA (SAOL) SANYO ELECTRIC CO LTD
CYC 1
PI JP 08213544 A 19960820 (199643)* 6p
ADT JP 08213544 A JP 1995-14296 19950131
PRAI JP 1995-14296 19950131
AB JP 08213544 A UPAB: 19961025
The appts. (1) has a metal substrate (3) in which an insulated layer is provided. An electrically-conductive material, e.g. wiring, a metal substrate, a pad, and a lead terminal, is provided on the insulated layer. An electric-conductive circuit **electrically connects** a **passive component** and/or active component.

A lead terminal is provided at the opposite side edge of the metal substrate **connected electrically** to an external lead terminal. The metal substrate is positioned in a way that it passes into the regular-interval inner side from an opposite side edge. The installation surface of the metal substrate is bent forming a U-shape.

ADVANTAGE - Provides easy design of printed **circuit board** including hybrid-integrated-circuit appts. Prevents external noise from infiltrating into circuit inside appts. Prevents circuit fracture generated when metal substrate is bent.
Dwg.1/6

L22 ANSWER 21 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1996-066659 [07] WPIX
DNN N1996-056136
TI Hybrid-integrated-circuit shielding structure device for thin shape

leadless surface mounting - has electrically conductive shielding pattern which covers sealing resin surface and ground pattern surface which is formed by printing.

DC U11 U14 V04
IN EGAWA, H
PA (NIDE) NEC CORP
CYC 2
PI JP 07326688 A 19951212 (199607)* 5p
US 5668406 A 19970916 (199743) 6p
ADT JP 07326688 A JP 1994-119114 19940531; US 5668406 A Cont of US 1995-455997 19950531, US 1996-767635 19961217
PRAI JP 1994-119114 19940531
AB JP 07326688 A UPAB: 19960222
The device comprises a recess (101) of a wiring board (11) which mounts an integrated-circuit chip (12) and a **passive-component** chip (19). The recess is sealed by a non-conductive sealing resin (13) after a bonding wire (8), a solder, a bump or an electrically conductive adhesive agent, connects the chip and a part of a wiring board inner-conductive layer (9).

Moreover, the chip is connected to an end-surface electrode (17), through the **bonding** wire. An **electrically** conductive shielding pattern (14) covers the sealing resin surface and the surface of a ground pattern (16) which is formed on the wiring board main side.

ADVANTAGE - Prevents severe effect of wave interference due to noise radiation generated by IC. Does not impair design freedom of **motherboard** since shielding pattern for **motherboard** is not needed.

Dwg.2/5

L22 ANSWER 22 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1995-116356 [16] WPIX
DNN N1995-091803
TI Power semiconductor component mounting system - uses similar spray coating process to apply **non-conductive ceramics** layer and overlying metal layer to power semiconductor.
DC V04
IN RAU, M; SCHAEFER, U; WEBER, D
PA (BOSC) BOSCH GMBH ROBERT
CYC 1
PI DE 4330975 A1 19950316 (199516)* 4p
DE 4330975 C2 20011025 (200164)
ADT DE 4330975 A1 DE 1993-4330975 19930913; DE 4330975 C2 DE 1993-4330975 19930913
PRAI DE 1993-4330975 19930913
AB DE 4330975 A UPAB: 19950502
The mounting system uses a thermic spray process to coat the surface (12) of the power semiconductor component (10) to be mounted on the **circuit board** (11) with a **non-conductive ceramics** layer (13). A similar process is used to apply a heat-conductive metal layer (14), which is soldered to the **circuit board** via a solder mass.

Pref. a plasma spray coating process, an arc spray coating process, or a flame spray coating process is used to apply each of the layers. The metal layer is pref. soldered to the **circuit board** via a solder paste (15), using a reflow soldering process.

ADVANTAGE - Good heat transfer characteristics between power semiconductor element and **circuit board** and hence to heat sink.

Dwg.1/1

L22 ANSWER 23 OF 28 WPIX (C) 2003 THOMSON DERWENT

AN 1994-076326 [10] WPIX
DNN N1994-059655
TI Printed circuit for high frequency applications - has aluminium-zinc alloy casing with supporting pins engaging holes in pcb and having their extremities soldered to surrounding conducting paths.
DC V04 W02
IN CHANTEAU, P
PA (PHIG) PHILIPS ELECTRONICS NV; (PHIG) PHILIPS ELECTRONIQUE GRAND PUBLIC; (PHIG) US PHILIPS CORP
CYC 7
PI EP 586010 A1 19940309 (199410)* FR 5p
FR 2695290 A1 19940304 (199415)
JP 06224571 A 19940812 (199437) 4p
US 5408207 A 19950418 (199521) 5p
EP 586010 B1 19961211 (199703) FR 6p
R: AT DE FR GB IT
DE 69306507 E 19970123 (199709)
ADT EP 586010 A1 EP 1993-202495 19930825; FR 2695290 A1 FR 1992-10480 19920902; JP 06224571 A JP 1993-214197 19930830; US 5408207 A US 1993-115336 19930901; EP 586010 B1 EP 1993-202495 19930825; DE 69306507 E DE 1993-606507 19930825, EP 1993-202495 19930825
FDT DE 69306507 E Based on EP 586010
PRAI FR 1992-10480 19920902
AB EP 586010 A UPAB: 19940421
The printed circuit includes a casing (1), moulded in an aluminium and zinc alloy, and housing a pcb (2) with one metallised surface (10). The pcb rests on pins (3) whose extremities engage holes provided on the pcb.
The holes are surrounded by circular conducting paths which are soldered to the pin extremities. All the earth connections on the pcb run to the circular paths surrounding the pin extremities.
USE/ADVANTAGE - For high frequency applications eg distribution circuits for cable television. Uses standard materials giving good performance. Has higher resonance frequency and better overloading coefficient. Has simple mechanical structure.
Dwg.1/2

L22 ANSWER 24 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1991-178314 [24] WPIX
DNN N1991-136561 DNC C1991-076994
TI High density multi-chip package - with short dense chip interconnections and good external heat conduction.
DC A85 U11 U14
IN BECHTEL, R L; HIVELY, J W; THOMAS, M
PA (TACT-N) TACTICAL FABS INC
CYC 32
PI WO 9107777 A 19910530 (199124)*
RW: AT BE CH DE DK ES FR GB GR IT LU NL OA SE
W: AT AU BB BG BR CA CH DE DK ES FI GB GR HU JP KP KR LK LU MC MG MW NL NO RO SE SU
AU 9169663 A 19910613 (199137)
US 5182632 A 19930126 (199307) 23p
ADT US 5182632 A Cont of US 1989-440545 19891122, US 1991-804614 19911202
PRAI US 1989-440545 19891122
AB WO 9107777 A UPAB: 19930928
Multi chip packages, with a heat sink in thermal connection with IC chips, each of which has several input/output (I/O) pads, are claimed. In one form, the package has externally accessible conductors and an interconnect structure in which selected pads of one chip are connected to selected pads of another clip and selected pads are connected to selected access conductors. The interconnect structure is formed on a surface comparable in flatness to a semiconductor wafer surface or each chip is held in

thermal contact with the heat sink by an elastomeric member located between the chip and a package surface opposite the heat sink.

USE/ADVANTAGE - The packages provide extremely high density electrical interconnection between multiple chips, allow extremely short dense chip interconnection, provide good heat conduction from the chips to the package exterior, allow integration of thin film **passive components** within the packages, allow re-working and repair and can be mfd. cost-effectively using current technology. @(55pp Dwg.No.3A/9)@

L22 ANSWER 25 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1991-086819 [12] WPIX
CR 1988-316192 [45]; 1991-156168 [21]
DNN N1991-067110 DNC C1991-036872
TI Glass-ceramic coated metal substrates for electronics - comprises metal core coated with compsn. based on magnesia, alumina, silica and boron oxide.
DC L02 L03 M26 P73 U11 U14
IN BLAZEJ, D C; OBOODI, R
PA (ALLC) ALLIED-SIGNAL INC
CYC 1
PI US 4997698 A 19910305 (199112)*
ADT US 4997698 A US 1989-370930 19890623
PRAI US 1987-45930 19870504; US 1988-212759 19880629; US 1989-370930 19890623
AB US 4997698 A UPAB: 19940510
Substrate comprises a metal core coated with a 0.02-0.10 mm **non-conductive** glass **ceramic** layer of compsn. (in wt.%): 8-26% pref. 9-22% esp. 12-14% MgO; 10-49%, pref. 16-45%, esp. 30-35% Al2O3; 42-68% pref. 43-63% esp. 45-52% SiO2; and 1-15%, pref. 5-12% esp. 7-9% on MgO + Al2O3 + SiO2, of B2O3 and one or more of alkali(ne earth) oxides and ZnO.

USE/ADVANTAGE In mfr. of electronic substrates andm **circuit boards**. Substrates have a high temp. firing capability (850 deg.C) and are air fireable. They have a compatible thermal expansion, low dielectric constant, high strength and high thermal stress resistance. @(16pp Dwg.No.1/4)@
1/4

L22 ANSWER 26 OF 28 WPIX (C) 2003 THOMSON DERWENT
AN 1986-340928 [52] WPIX
DNN N1986-254424
TI Self-soldering, flexible circuit connector - has solder covering exposed conductors and heater on opposite face.
DC P55 V04
IN KENT, H B
PA (METC-N) METCAL INC
CYC 13
PI EP 206619 A 19861230 (198652)* EN 32p
R: AT BE CH DE FR GB IT LI NL SE
JP 61294778 A 19861225 (198706)
US 4788404 A 19881129 (198850)
CA 1255012 A 19890530 (198926)
CA 1264378 A 19900109 (199006)
US 5045666 A 19910903 (199138)
EP 206619 B1 19930120 (199303) EN 20p
R: AT BE CH DE FR GB IT LI NL SE
US 5175409 A 19921229 (199303) 13p
DE 3687546 G 19930304 (199310)
ADT EP 206619 A EP 1986-304393 19860609; JP 61294778 A JP 1986-145977 19860620; US 4788404 A US 1985-746796 19850620; US 5045666 A US

1990-515333 19900430; EP 206619 B1 EP 1986-304393 19860609; US 5175409 A Div ex US 1985-746796 19850620, Cont of US 1988-252738 19881003, Cont of US 1990-515333 19900430, US 1990-626534 19901212; DE 3687546 G DE 1986-3687546 19860609, EP 1986-304393 19860609

FDT US 5175409 A Div ex US 4788404, Cont of US 5045666; DE 3687546 G Based on EP 206619

PRAI US 1985-746796 19850620

AB EP 206619 A UPAB: 19930922

The flexible circuit is folded around a self-regulating heater formed of a bus (294), successively covered with an insulating layer (296), a ferromagnetic layer (298), and a copper layer (300). The circuit conductors are exposed on the face away from the heater by a gap in the circuit insulation.

A solder reflow pad is formed by a window in an insulating layer (304), the window coinciding with the gap in the circuit insulation and being filled with solder (308) to form a connection, e.g. with a printed **circuit board**, upon heating.

ADVANTAGE - Combines high density capability with reliability of soldered joint. Heater also permits temporary bonding of circuit to metal plate, to prevent corrosion of exposed solder contacts during storage. 19/19

L22 ANSWER 27 OF 28 JAPIO COPYRIGHT 2003 JPO

AN 2002-076637 JAPIO

TI SUBSTRATE INCORPORATING CHIP COMPONENT, AND MANUFACTURING METHOD OF THE SUBSTRATE

IN SUGAYA YASUHIRO; ASAHI TOSHIYUKI; KOMATSU SHINGO; NAKATANI SEIICHI

PA MATSUSHITA ELECTRIC IND CO LTD

PI JP 2002076637 A 20020315 Heisei

AI JP 2000-259419 (JP2000259419 Heisei) 20000829

PRAI JP 2000-259419 20000829

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002

AB PROBLEM TO BE SOLVED: To provide a component configuration for reducing a packaging surface and thinning the thickness of a film incorporating components when incorporating the chip component into a substrate, and manufacturing method for accurately packaging and incorporating such chip **passive component** as an LCR by forming a fine wiring pattern on a **circuit board** and at the same time forming the connection with the wiring pattern.
SOLUTION: An electrode is formed at least at either an upper or lower surface, at least one chip component is incorporated, a thickness (t) of the chip passive element 204 is smaller than length L and width W, the chip components have an external connection electrode 204 at least at one of surfaces corresponding to the upper and lower surfaces to the thickness direction, and the external connection electrode 205 is **electrically connected** to the wiring pattern 203 formed at an electrically insulated multilayer interconnection board 201.

L22 ANSWER 28 OF 28 JAPIO COPYRIGHT 2003 JPO

AN 2002-026635 JAPIO

TI PLANAR ANTENNA SYSTEM

IN YAMAMOTO HIROYASU

PA IWAKI ELECTRONICS CORP

PI JP 2002026635 A 20020125 Heisei

AI JP 2000-211038 (JP2000211038 Heisei) 20000712

PRAI JP 2000-211038 20000712

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002

AB PROBLEM TO BE SOLVED: To provide a planar antenna system that realizes downsizing, high reliability, low cost and automatic assembling.
SOLUTION: The planar antenna system A is configured with an antenna

element 1 in which a reception electrode 3 and a ground electrode is formed and with a printed **circuit board** 5 that is placed on a lower side of the ground electrode and on which a high frequency amplifier, a SAW filter and a reception control circuit or the like are mounted. A feeding terminal **electrically connected** to the reception electrode 3 is formed on a ground electrode face of the antenna element 1. A pair-chip element is mounted on the side of the printed **circuit board** 5 toward the ground electrode side, the pair-chip element subjected to air-tight sealing and **electric** shield is **connected** to the ground electrode face with a conductor, and a feeding pad on the board face is **electrically connected** to the reception electrode 3 via the feeding terminal. Furthermore, circuit components such as **passive components** and semiconductor components are mounted on the opposite side to the printed **circuit board** 5 and electric shield is applied to the component mount side.

L23 ANSWER 1 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 2002-337641 [37] WPIX
CR 2000-580715 [55]
DNN N2002-265296 DNC C2002-097109
TI Adhesive composition for use in micro-electronic device, comprises polymeric resin, conductive filler, corrosion inhibitor which is 8-hydroxyquinoline, and optional component such as diluent, filler, adhesion promoter.
DC A85 E13 L03 X12
IN CHENG, C; FREDRICKSON, G; LU, D; TONG, Q K; XIAO, Y
PA (NATT) NAT STARCH & CHEM INVESTMENT HOLDING COR
CYC 27
PI US 6344157 B1 20020205 (200237)* 13p
EP 1231248 A1 20020814 (200261) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
ADT US 6344157 B1 CIP of US 1999-249927 19990212, US 2001-782421 20010213; EP 1231248 A1 EP 2002-2060 20020208
PRAI US 2001-782421 20010213; US 1999-249927 19990212
AB US 6344157 B UPAB: 20020924
NOVELTY - A composition for use in microelectronic devices comprises a polymeric resin, a conductive filler, a corrosion inhibitor, optionally a reactive or a non-reactive diluent, optionally an inert filler and optionally an adhesion promoter. The corrosion inhibitor is 8-hydroxyquinoline.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of enhancing the electrical stability of the composition which involves adding the corrosion inhibitor and the low melting point metal filler to the composition.

USE - Useful as **conductive** or **resistive** material in microelectronic devices or semiconductor packages. The conductive adhesives are used to bond integrated chips to substrates or circuit assemblies to printed wire boards, and for forming planar or buried resistors in **circuit boards**.

ADVANTAGE - The composition comprising corrosion inhibitor and low melting point metal exhibits improved electrical stability, conductive stability, and high contact resistance when exposed to harsh environmental conditions.

DESCRIPTION OF DRAWING(S) - The figure is a graph showing effect of oxygen scavengers on the contact resistivity of the composition after exposure to 85 deg. C and 85% RH for 500 hours.
Dwg.1/5

L23 ANSWER 2 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 2002-033279 [04] WPIX
DNN N2002-025541 DNC C2002-009271
TI Securing method of thin film material for conveyorized processing, involves adhering thin film to adhesive pattern formed on rigid carrier, adhering photoresist on thin film, exposing to patterned actinic radiation.
DC G06 L03 P83 P84 V04
IN CARPENTER, R W
PA (MORN) MORTON INT INC
CYC 29
PI US 6309805 B1 20011030 (200204)* 5p
EP 1198161 A1 20020417 (200233)# EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2002134877 A 20020510 (200246)# 14p
CN 1349375 A 20020515 (200260)#

KR 2002029689 A 20020419 (200269)#
ADT US 6309805 B1 US 1999-388308 19990901; EP 1198161 A1 EP 2000-308917 20001010; JP 2002134877 A JP 2000-309809 20001010; CN 1349375 A CN 2000-134403 20001017; KR 2002029689 A KR 2000-60291 20001013
PRAI US 1999-388308 19990901; EP 2000-308917 20001010; JP 2000-309809 20001010; CN 2000-134403 20001017; KR 2000-60291 20001013
AB US 6309805 B UPAB: 20020117
NOVELTY - An adhesive pattern (AP) (to adhere periphery of thin film (TF)) is formed on rigid carrier, TF is adhered to AP and photoresist layer (PL) is applied on TF so that PL extends over exposed perimeter of carrier. PL is then exposed to patterned actinic radiation so that during development, perimeter of PL remains over that of carrier and extends inward over periphery of TF to secure TF during processing.

DETAILED DESCRIPTION - The rigid carrier (11) has dimensions greater than that of thin film (10). The thin film is placed on surface of the carrier, leaving the perimeter of the carrier exposed. The adhesive (12) is selected to have greater adhesion to carrier surface than to thin film and has sufficiently low adhesion to thin film such that thin film may later be peeled from adhesive pattern without damage to the thin film. The actinic radiation is patterned to sufficiently secure the thin film during subsequent processing.

USE - For securing thin film material for conveyorized processing. The thin film material is used to form embedded electrical components such as capacitors and resistors of multi-layer printed **circuit boards**.

ADVANTAGE - The thin film material is processed through aggressive chemical handling equipment without damage and with minimum handling. The securing method is applicable to the formation of thin film capacitors and resistors.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of the etched thin film laminated to rigid layer.
Thin film 10
Rigid support 11
Adhesive pattern 12
Perimeter region of carrier 15
Photoresist layer 17
Dwg.5/6

L23 ANSWER 3 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 2001-514337 [56] WPIX
DNN N2001-381038
TI Keypad structure for use in a keyboard, uses capacitive coupling to detect keypad depression.
DC T04 U21 V03
IN KAIKURANTA, T; SALMINEN, S; SVARFVAR, B; VUORI, P
PA (OYNO) NOKIA MOBILE PHONES LTD; (OYNO) NOKIA CORP
CYC 95
PI WO 2001048771 A1 20010705 (200156)* EN 36p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
FI 9902794 A 20010629 (200156)
AU 2001025198 A 20010709 (200164)
FI 108096 B1 20011115 (200176)
US 2002093489 A1 20020718 (200254)
EP 1243009 A1 20020925 (200271) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

ADT WO 2001048771 A1 WO 2000-FI1152 20001228; FI 9902794 A FI 1999-2794 19991228; AU 2001025198 A AU 2001-25198 20001228; FI 108096 B1 FI 1999-2794 19991228; US 2002093489 A1 US 2000-746464 20001221; EP 1243009 A1 EP 2000-988841 20001228, WO 2000-FI1152 20001228
FDT AU 2001025198 A Based on WO 200148771; FI 108096 B1 Previous Publ. FI 9902794; EP 1243009 A1 Based on WO 200148771
PRAI FI 1999-2794 19991228
AB WO 200148771 A UPAB: 20011001
NOVELTY - Insulating film (702) separates resistive strip ends (709,710) from corresponding conductive input pads (706,708) respectively and dome sheet contact (711) from output pad (707). Perforated insulating film (704) separates the resistive strip (703) from dome sheet (705) so that depression of a dome by its associated key will cause a related proportion of an alternating input signal to be passed to the output via the capacitively coupled input and output pads.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) an exchangeable cover;

(b) an electronic device including a keypad.

USE - For use in keyboard structures, particularly keyboards of the kind that appear in portable telecommunications devices such as mobile telephones, multi-function communicators, portable digital assistants and palmtop computers.

ADVANTAGE - The capacitively coupled keypad places few limitations on the layout design of both the printed **circuit board** and the appearance of the keypad, the three dimensional design of the keypad is freed from the planarity of the printed **circuit board** and the location, number and size of keys is independent of PCB layout. Realization of watertight or even hermetically sealed keypad-controlled devices becomes easier, key pad indications can be transmitted through moveable joints between device parts and a great degree of freedom is given to the design of exchangeable outer covers. In many cases the conductive dome sheet can function as a part of electromagnetic interference shielding which can reduce the overall component count, reducing manufacturing cost and structural complexity.

DESCRIPTION OF DRAWING(S) - The figure illustrates a capacitively coupled keypad structure.

Insulating film ((703) Meandering resistive strip ((704) Perforated insulating film ((705) Conductive dome sheet ((706,708) Conductive input pads ((707) Conductive output pad ((709,710) Ends of meandering **resistive** strip ((711) **Conductive** tab of dome sheet.

702

Dwg.7/18

L23 ANSWER 4 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 2001-023002 [03] WPIX
CR 1999-095045 [08]; 2000-072090 [06]
DNN N2001-017882 DNC C2001-006836
TI Making electrical connection to electrical device involves depositing bumps of polymeric base composite on bonding pads, drying the bumps, and pressing on the substrate.
DC A85 L03 U11 V04
IN ROLDAN, J M; SARAF, R F
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6127253 A 20001003 (200103)* 12p
ADT US 6127253 A Div ex US 1996-693923 19960805, US 1998-134210 19980814
FDT US 6127253 A Div ex US 5854514
PRAI US 1996-693923 19960805; US 1998-134210 19980814
AB US 6127253 A UPAB: 20010116
NOVELTY - An electrical connection to an electrical device is made by

depositing bumps of a polymeric based composite on bonding pads of an electrical device; drying the bumps; and pressing the bumps against a substrate with an electrically conductive surface (32) together mechanically under a pressure to establish electrical connection between the bumps and the conductive surface on the substrate.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of removing an electrical interconnection between a first composite and an electrically conductive surface on a substrate by removing a pressure exerted on the composite against the conductive surface on the substrate.

USE - For making an electrical connection to an electrical device (12).

ADVANTAGE - The bumps are reworkable after being bonded to a substrate or another electronic device. They are compliant, elastic, and pliable when compared to conventional solder bumps so that highly reliable interconnections to another electronic device. The conductivity of the conductive bumps is found to be equal to or better than solder and they are resilient to thermal cycle and moisture exposure in environmental and functional testing. The interconnection can be easily disassembled by simply removing the load and dismantling the assembly to recover the electronic devices.

DESCRIPTION OF DRAWING(S) - The figure shows an enlarged cross-sectional view of the invention.

Electrical device 12
Bumps 22
Bonding pads 28
Electrically conductive surface 32
Dwg.1D/7

L23 ANSWER 5 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 2000-580715 [55] WPIX
CR 2002-337641 [21]
DNN N2000-429846 DNC C2000-172977
TI **Conductive** and **resistive** material for use in microelectronic devices, includes oxygen scavenger and/or corrosion inhibitor to provide electrical stability.
DC A14 A21 A26 A85 E19 L03 U11 U12
IN LU, D; TONG, Q; YUE XIAO, A
PA (NATT) NAT STARCH & CHEM INVESTMENT HOLDING COR
CYC 28
PI EP 1032038 A2 20000830 (200055)* EN 11p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000273317 A 20001003 (200056) 30p
CN 1267891 A 20000927 (200067)
KR 2000058019 A 20000925 (200122)
ADT EP 1032038 A2 EP 2000-102225 20000211; JP 2000273317 A JP 2000-33208 20000210; CN 1267891 A CN 2000-104862 20000211; KR 2000058019 A KR 2000-6470 20000211
PRAI US 1999-249927 19990212
AB EP 1032038 A UPAB: 20020613
NOVELTY - Oxygen scavengers and/or corrosion inhibitors are included in a polymeric resin composition comprising a conductive filler, without significantly effecting the physical (**resistive** or **conductive**) properties of the resin when used for microelectronic devices.

DETAILED DESCRIPTION - A composition for use in microelectronic devices comprising:

(a) a polymeric resin;
(b) a conductive filler;
(c) a reactive or nonreactive diluent (optional);

(d) an inert filler (optional);
(e) an adhesion promoter (optional); and
(f) an oxygen scavenger and/or corrosion inhibitor.
An INDEPENDENT CLAIM is also included for a method of enhancing electrical stability of a composition by adding an oxygen scavenger and/or corrosion inhibitor.
USE - As **conductive** or **resistive** materials for fabrication and assembly of microelectronic devices or semiconductor packages e.g. as conductive adhesive for bonding integrated circuits to substrates or as resist material to form planar or buried resistors in **circuit boards**.
ADVANTAGE - Compositions provide electrically stable interconnections without significantly reducing **conductive** or **resistive** properties.
Dwg.0/4

L23 ANSWER 6 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 2000-183316 [16] WPIX
DNN N2000-135164 DNC C2000-057608
TI Electrically resistive composite material for the manufacture of integral **circuit board** components has a conductive and a non-conductive material.
DC A85 L03 V01
IN CARBIN, D; MEIGS, J H
PA (ALLC) ALLIED-SIGNAL INC; (OAKN) OAK-MITSUI INC
CYC 82
PI WO 2000007197 A2 20000210 (200016)* EN 25p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
AU 9952340 A 20000221 (200029)
EP 1145256 A2 20011017 (200169) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
KR 2001071075 A 20010728 (200208)
CN 1352870 A 20020605 (200261)
ADT WO 2000007197 A2 WO 1999-US16980 19990728; AU 9952340 A AU 1999-52340 19990728; EP 1145256 A2 EP 1999-937526 19990728, WO 1999-US16980 19990728; KR 2001071075 A KR 2001-701290 20010130; CN 1352870 A CN 1999-809185 19990728
FDT AU 9952340 A Based on WO 200007197; EP 1145256 A2 Based on WO 200007197
PRAI US 1999-361458 19990727; US 1998-94746P 19980731
AB WO 200007197 A UPAB: 20000330
NOVELTY - An electrically resistive composite material (12) for integral **circuit board** components comprises a conductive and a non-conductive material.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for: (A) a multilayer foil comprising a conductive metal layer and a layer of electrically resistive composite material; (B) a **circuit board** having an integral resistor; and (C) a method of manufacturing a printed **circuit board**. The **circuit board** comprises (a) an insulative substrate layer (14) having two surfaces; (b) an integral resistor; and (c) first and second conductive metal layers (10). The method (C) includes (i) applying a first photosensitive etch resistant material to a laminate having an insulative substrate, a conductive metal layer and a resistive material layer; (ii) irradiating a portion of the photosensitive etch resistant material; (iii) removing a portion of the photosensitive etch resistant material to expose a portion of the conductive metal layer; (iv)

removing the **conductive** metal and **resistive** material layers to form a partially formed integral resistor; (v) removing the photosensitive etch resistant material from the partially formed integral resistor; (vi) applying and masking a second photosensitive etch resistant material, and irradiating its unmasked portions to form an integral resistor; and (vii) removing the photosensitive etch resistant material and the conductive layer to form the integral resistor.

USE - The resistive composite is used in the manufacture of integral **circuit board** components.

ADVANTAGE - The composite material can be manufactured into a resistive layer that is thick enough to withstand incidental damage during manufacturing processes. The ingredient ratios of the composite material can be varied and formed into resistive foils that have a uniform thickness but with varying sheet resistivities, and this allows for more uniformity in the manufacture of **circuit board** components. The resistive layer of composite material is also less prone to resistive variations due to physical damage.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an integral resistor.

Conductive metal layer 10
Resistive composite material or co-deposit layer 12
Substrate layer 14
Non-conductive particles or particulate material 36

Dwg.9/9

L23 ANSWER 7 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1999-603218 [52] WPIX
CR 2002-572856 [61]
DNN N1999-444851 DNC C1999-175717
TI Fabrication of thin film resistors embedded into printed **circuit boards**.
DC E11 E12 L03 V01 V04
IN BOTTOMLEY, S E; CARPENTER, R W; HENDRICK, M; HUNT, A T; HWANG, T J; LIN, W; LUTEN, H A; MCENTYRE, J E; SHAO, H; SHOUP, S S; THOMAS, J; TZYY, J H; HORNIS, H G
PA (MICR-N) MICROCOATING TECHNOLOGIES INC; (MORN) MORTON INT INC; (MORN) MORTON INT CO LTD; (MORN) MORTON INT
CYC 33
PI EP 955642 A2 19991110 (199952)* EN 43p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
SG 68713 A1 19991116 (199954)
JP 11340003 A 19991210 (200009) 37p
CN 1234588 A 19991110 (200012)
CA 2267492 A1 19991029 (200014) EN
KR 99083589 A 19991125 (200055)
MX 9903700 A1 19991101 (200106)
US 6193911 B1 20010227 (200114)
US 6208234 B1 20010327 (200119)
US 6210592 B1 20010403 (200120)
BR 9901357 A 20010320 (200123)
US 6329899 B1 20011211 (200204)
KR 322287 B 20020325 (200265)
ADT EP 955642 A2 EP 1999-303244 19990427; SG 68713 A1 SG 1999-1670 19990414; JP 11340003 A JP 1999-124575 19990430; CN 1234588 A CN 1999-106358 19990429; CA 2267492 A1 CA 1999-2267492 19990329; KR 99083589 A KR 1999-15362 19990429; MX 9903700 A1 MX 1999-3700 19990421; US 6193911 B1 US 1998-69640 19980429; US 6208234 B1 US 1998-69427 19980429; US 6210592 B1 US 1998-69679 19980429; BR 9901357 A BR 1999-1357 19990428; US 6329899 B1 CIP of US 1998-69679 19980429, US 1998-198954 19981124; KR 322287 B KR 1999-15362 19990429

FDT US 6329899 B1 CIP of US 6210592; KR 322287 B Previous Publ. KR 99083589
PRAI US 1998-198954 19981124; US 1998-69427 19980429; US 1998-69640 19980429; US 1998-69679 19980429

AB EP 955642 A UPAB: 20021010
NOVELTY - A combination of gas combustion chemical vapor deposition and masking and etching processes is used in the formation of thin film resistors embedded into printed **circuit boards**. This avoids damage to thermally sensitive substrates and among others metallic nickel coatings can be formed onto polyimide sheet without deformation.

DETAILED DESCRIPTION - (A) Precursor solution for forming an electrically resistive material comprising a homogenous mixture of conducting metal and a metal oxide or metalloid oxide. The solution comprises: (a) first precursor chemical which when subjected to either flame combustion or controlled atmospheric combustion vapor deposition yields a zero valent metal; (b) second precursor yields a metal oxide and a metalloid oxide; (c) one or more solvents. The first and second precursors are mutually soluble and are present in the solvent at 0.005 - 20 wt.%.

INDEPENDENT CLAIMS are also included for:

(B) Precursor solution containing non-oxygen element precursors which yield a conductive metal oxide having sufficient electrical resistivity to be used as a resistor under flame combustion conditions;

(C) Precursor solution as (B) which yields bismuth ruthenate $BiRu_2O_7$ or strontium ruthenate $SrRuO_3$, the first precursor containing Bi or Sr and the second Ru;

(D) Precursor solution comprising at most 40 wt.% water, 60 - 100 wt.% liquefied ammonia or N_2O as a solvent, and 0.001-0.1 wt.% total nickel or nickel plus dopant precursors which yield nickel or doped nickel deposit;

(E) Method of forming a discrete electrical resistor by: (a) Providing a layer of resistive material comprising a homogenous mixture of noble metal and dielectric material on an insulating substrate; (b) Covering selected portions of the layer with a photoresist which is inert to aqua regia; (c) Etching the layer with aqua regia so as to leave a patch and then providing connection from the patch to electronic circuitry;

(F) Method as (E) to create a patch of resistive material and a number of patches of conductive material in electrical contact with it at spaced apart locations, in which a three layer structure of substrate - **resistive** material - **conductive** material is formed and etched with aqua regia using a photoresist mask to form the patches and the selectively etched to remove metal and not resistor to form the contacts, and (F) in which the metal is patterned before the patches are etched;

(G) Method of forming a patterned layer of resistive material in electrical contact with a layer of electrically conductive material by; (a) Providing a three layer structure of metal conductor, chemically etchable intermediate layer, porous resistive material layer allowing the chemical etchant to penetrate and etch the intermediate layer. (b) Forming a patterned layer of photoresist and exposing the resistive material to chemical etchant. (c) Forming a pattern by ablating away the resistive layer in the regions where the intermediate layer was etched;

(H) The method in which: (a) A layer of resistive material comprising zero valence metal or alloy is formed on an insulating substrate and then covered with a layer of conductive material, and then patterned photoresist. (b) Etching the structure to remove exposed conductor and underlying resistive material. (c) Removing the photoresist and covering with a second patterned photoresist. (d) Etching exposed conductor with second etch which does not etch the underlying resistive material;

(I) The method as (H) in which the conductive layer is provided and patterned over the resistive material after it has been etched into

patches.

(J) The methods as above when used to form ruthenate resistors using precursor (C);

(K) The method in which; (a) Resistive material is formed on a metal foil. (b) Patterned photoresist is formed and exposed resistive material etched away from the foil. (c) Photoresist removed and a sheet of polymer laminated to the resistive layer side. (d) Metal foil covered with patterned photoresist and exposed foil etched away. Also included are the resistors and two and three layer structures made by the claimed methods using the claimed precursors

USE - Thin film resistors in printed **circuit boards**

ADVANTAGE - The resistors can be embedded in the **circuit board** without heating the board and degrading polymeric materials.

DESCRIPTION OF DRAWING(S) - The drawing shows a resistor structure.

Thin resistive layer 401

Insulating substrate 402

Copper connectors 403

Insulating layers 420

Dwg.6/10

L23 ANSWER 8 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1999-312510 [26] WPIX
DNN N1999-233402
TI Multi speed multi direction analog pad pointing device for computers, remote controls, and web TV.
DC T04 V01 V03 W03 W04 W05
IN DEVOLPI, D R
PA (DEVO-I) DEVOLPI D R
CYC 84
PI WO 9919887 A1 19990422 (199926)* EN 32p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
US 5912612 A 19990615 (199930)
AU 9897996 A 19990503 (199937)
US 6067005 A 20000523 (200032)
EP 1029331 A1 20000823 (200041) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
US 6107993 A 20000822 (200042)
US 6201468 B1 20010313 (200120)
ADT WO 9919887 A1 WO 1998-US21482 19981012; US 5912612 A Provisional US 1997-61825P 19971014, US 1998-96301 19980531; AU 9897996 A AU 1998-97996 19981012; US 6067005 A Provisional US 1997-61825P 19971014, CIP of US 1998-96301 19980531, US 1999-307581 19990507; EP 1029331 A1 EP 1998-952248 19981012, WO 1998-US21482 19981012; US 6107993 A Provisional US 1997-61825P 19971014, US 1998-88184 19980601; US 6201468 B1 Provisional US 1997-61825P 19971014, CIP of US 1998-88184 19980601, US 2000-643153 20000821
FDT AU 9897996 A Based on WO 9919887; US 6067005 A CIP of US 5912612; EP 1029331 A1 Based on WO 9919887; US 6201468 B1 CIP of US 6107993
PRAI US 1998-96301 19980531; US 1997-61825P 19971014; US 1999-307581 19990507; US 1998-88184 19980601; US 2000-643153 20000821
AB WO 9919887 A UPAB: 19990723
NOVELTY - Pad pointing device comprises a top cover (10) with a protruding plus shaped segment (18) formed on its bottom surface. The segment is shaped with a number of ribs which radiate out from its center at various angles and is made of an elastic material. The lower surface of the

segment is electrically **conductive** or **resistive**. The top cover is formed with an elastic return ridge (16) that encircles the segment (18). The device also includes a substrate (20) such as a printed **circuit board** which has electrically connected resistive regions (22) and conductive regions (24). When an external force is applied, the return ridge deforms, the plus shaped segment moves downward and tilts in orientation so that contact is made with the substrate **conductive** or **resistive** tracts in a location corresponding to the direction and degree of the applied force. The output signal can be translated by analog to digital or RC timing circuitry into speed and direction vectors.

USE - As a cursor pointing device for computers, remote controls, web TV, TV guide browsers, video games, consumer electronics, industrial controllers, medical, automotive and other applications.

ADVANTAGE - Device has improved performance, reliability and durability and can be mass produced.

Dwg.1/16

L23 ANSWER 9 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1997-558755 [51] WPIX
DNN N1997-465712 DNC C1997-178399
TI Electroformed squeegee blade - has electroformed edge which contacts stencil to squeeze printing material through onto substrate.
DC A88 L03 M11 P42 P74 P75
IN FISCHBECK, K W; MARKS, G T
PA (AMTX-N) AMTX INC; (XERO) XEROX CORP
CYC 77
PI WO 9741969 A1 19971113 (199751)* EN 22p
RW: AT BE CH DE DK EA ES FI FR GB GH GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN YU
AU 9729335 A 19971126 (199813)
US 5746127 A 19980505 (199825)
EP 1015130 A1 20000705 (200035) EN
R: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
EP 1015130 B1 20021120 (200277) EN
R: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
ADT WO 9741969 A1 WO 1997-US7630 19970505; AU 9729335 A AU 1997-29335 19970505; US 5746127 A US 1996-646380 19960503; EP 1015130 A1 EP 1997-923561 19970505, WO 1997-US7630 19970505; EP 1015130 B1 EP 1997-923561 19970505, WO 1997-US7630 19970505
FDT AU 9729335 A Based on WO 9741969; EP 1015130 A1 Based on WO 9741969; EP 1015130 B1 Based on WO 9741969
PRAI US 1996-646380 19960503
AB WO 9741969 A UPAB: 19971222
A squeegee blade has an electroformed layer of material selected from: Ni, Cu, Au, Ag, Pd, Sn, Pb, Cr, Zn, Co, Fe, their alloys, Ni-P, Ni-B, Cu-Ni-P, Ni-PTFE and their composites.

Also claimed are:

(1) manufacturing the blade by patterning a conductive substrate core with a photoresist in the form of a squeegee blade and electroforming the material onto the core, and

(2) the method and apparatus for deposition of printing material onto a substrate by placing a stencil in contact with a substrate, depositing printing material onto the stencil, and moving the squeegee blade across the stencil to spread the printing material and deposit it on the substrate.

The electroformed layer is of Cu or Ni.

Solder paste is used as the printing material applied on a PWB

substrate.

USE - Used in the deposition of printing material onto printed **circuit boards** and printed wiring boards, as well as in screen printing of solder paste, **conductive** epoxies, **conductive/resistive** inks, etc., in the fabrication of various electronic assemblies.

ADVANTAGE - Various blade edge designs and thicknesses can be produced that allow for user definable printing characteristics to be prepared. Multiple layer designs can be manufactured. Secondary processing, additional finishing, and speciality coating or plating are eliminated. Smooth, flat surfaces can be formed without lapping or grinding and the blade is more compatible with stencil materials due to increased lubricity between the blade and stencil.

Dwg.4/4

L23 ANSWER 10 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1997-434274 [40] WPIX
DNN N1997-361302
TI Spreading apparatus for paste substance on **circuit board** - has locking device including pair of oppositely-disposed, arch-shaped locking clamps which fixes angle of blade relative to **circuit board**.
DC P42 U14 V04 X24
IN ENTERKIN, R J; HOWE, G K; VOLPE, J J
PA (JNJI-N) JNJ IND INC
CYC 1
PI US 5660632 A 19970826 (199740)* 9p
ADT US 5660632 A US 1995-572971 19951215
PRAI US 1995-572971 19951215
AB US 5660632 A UPAB: 19971006

The apparatus (10) comprises a housing (18) having a groove (20), extending through it, which is coequal in length with the housing. An elongated shaft (12), having a longitudinal slot (14) coequal in length with it, is disposed within the groove for selective rotation in it. An elongated blade (16), mounted to the slot of the shaft, is rotatable concomitant with the rotation of the shaft in order to adjust the angle between the blade and the **circuit board**. A locking device, attachable to the housing, fixes the angle of the blade relative to the **circuit board**.

The locking device includes a pair of oppositely-disposed, arch-shaped locking clamps (22) mounted to the ends of the housing so that they can be selectively compressed against the shaft to prevent shaft rotation within the housing. Each locking clamp further includes a main body portion (28) and a pair of oppositely-disposed legs (30), defining an aperture (32) for receiving the shaft, and which contact the shaft for preventing shaft rotation within the housing.

USE/ADVANTAGE - For screen and stencil printing solder paste, epoxies, **conductive** inks, **resistive** inks and dielectric inks onto PCBs in surface mount technology. Incorporates adjustable 'angle of attack' in its design. Readily adaptable to various squeegee blade holders and squeegee head assemblies.

Dwg.1/14

L23 ANSWER 11 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1996-467225 [47] WPIX
DNN N1996-393547
TI Electrical circuit assembly - has **conductive** track with **resistive** nature close in thermal proximity to electrical component and voltage across track causing resistive region to increase in temp to heat electrical component.
DC U11 V04

01/06/2003

IN MCCANN, M O
PA (SMIS) SMITHS IND PLC
CYC 2
PI GB 2300340 A 19961030 (199647)* 10p
DE 19608858 A1 19961031 (199649) 5p
ADT GB 2300340 A GB 1996-3041 19960214; DE 19608858 A1 DE 1996-19608858 19960307
PRAI GB 1995-8631 19950428
AB GB 2300340 A UPAB: 19961124
The circuit includes a **circuit board** (10) supporting electrical components (11 to 15) and at least one conductive track (20) formed of a lower layer (17) of nickel, having a high resistivity and an upper layer (18) of copper with a low resistivity. The track (20) is connected at opposite ends to a power supply (15) and has its copper layer (18) removed in a region (30) where the track extends beneath one of the components (11).

A voltage applied across the track causes resistive heating of the region and hence of the component above the region. A thermostat (12) and a safety cut-out (13) are connected in series in the track (20) to prevent current flow along the track when the temperature rises above a predetermined value or when current exceeds a predetermined value.

USE/ADVANTAGE - For VRAM. Avoids need of separate heaters.

Dwg.1,2/2

L23 ANSWER 12 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1996-159621 [16] WPIX
DNN N1996-133830 DNC C1996-050306
TI Mfg. printed wiring boards with reduced number of operations - using combination of plasma etch back-desmear, carbon coating, and panel electroplating.
DC L03 P78 V04
IN DURGIN, D L; HOKE, R T; MALINS, R J
PA (QUAT-N) QUATRO CORP
CYC 1
PI US 5498311 A 19960312 (199616)* 6p
ADT US 5498311 A US 1994-260746 19940615
PRAI US 1994-260746 19940615
AB US 5498311 A UPAB: 19960422
A printed wiring board is made by imaging a copper laminated board coated with an organic surface protectant by applying a photoresist and exposing it, then developing, etching, and stripping the board, and adding at least one further copper laminated board to form a layered **circuit board**. The boards of the layered **circuit board** are pressed together and holes drilled at predetermined locations and deburred before performing a plasma desmear/etchback process, covering exposed surfaces with a non-metallic, less **resistive**/more **conductive** material, panel plating the board, copper surfaces, and covered surfaces, pretreating the panel plated board by abrading its copper surfaces, imaging the board again by applying photoresist and photographically exposing it, and developing, etching, and stripping the panel plated board.

Also claimed is a method of mfg. a printed wiring board in which the production of hazardous waste by-product is minimised or eliminated, where a laminated board is provided having non-conductive material interposed between two conductive metal layers and at least one formed hole extending between the conductive metal layers, desmear and etch back operations being performed on the hole using and oxygen and CF4 plasma gas mixture, a liquid dispersion of non-metallic, electrically conducting substance being applied to non-conductive and conductive metal surfaces, a continuous conductive metal layer being electroplated over the non-metallic substance, photoresist being applied to the outer surface of each

conductive metal layer to seal the at least one hole, unwanted copper being etched away from exposed conductive layers, and the photoresist being removed.

ADVANTAGE - The number of operations required to produce a complete, operational printed wiring board is reduced and the production of by-products contg. manganese, tin, and lead eliminated by combining plasma etch back/desmear, McDermid ''Black Hole'' (RTM) technology for carbon coating, and panel electroplating.

Dwg.1/2

L23 ANSWER 13 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1995-150067 [20] WPIX
DNN N1995-117777
TI Flexible circuit substrate for use in LCD, ECD and solar battery - incorporates hard oxide layer to fill up space between circuits and this layer is of UV ray hardening type ink.
DC U12 U14 V04 X12 X15
IN HATAKEYAMA, T; ISONO, T; MURATA, K; SHIBATA, M
PA (NIKO-N) NIPPON KOKUEN KOGYO KK; (NIGR-N) NIPPON GRAPHITE IND LTD
CYC 2
PI JP 07073739 A 19950317 (199520)* 7p
US 5493074 A 19960220 (199613) 9p
US 5603158 A 19970218 (199713) 9p
ADT JP 07073739 A JP 1993-220043 19930903; US 5493074 A US 1994-264781 19940623; US 5603158 A Div ex US 1994-264781 19940623, US 1995-554484 19951107
FDT US 5603158 A Div ex US 5493074
PRAI JP 1993-220043 19930903
AB JP 07073739 A UPAB: 19950530
The flexible circuit substrate (10) consists of an adhesive agent layer (2) which is provided over an insulation film (1). An electric conduction circuit (9) connecting a metal plate coating (5) is formed over this adhesive layer. The metal plate coating hides the surface of a metal foil (3A). The space between adjacent circuits is filled up with a hard oxide layer (8) of hardening type ink. The surface of the substrate is then smoothed.

At the time of manufacturing UV-ray hardening type ink is applied to the side of metal foil. The UV-ray hard coating film is formed by drying the substrate. The UV-ray hard coating film is stiffened in the space between electric conduction circuits. Development liquid removes the non-hardened portions of the oxide film.

USE/ADVANTAGE - For use in LCD pipe, ECD, solar battery, word processor, clock, camera etc. Connects electrode part and terminal part of PCB mechanically and electrically. Increases adhesion intensity of hot molten adhesive agent. Ensures stability improves reliability.

Dwg.3/3

L23 ANSWER 14 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1994-311469 [39] WPIX
DNN N1994-245210 DNC C1994-141517
TI Resistance used in surface mounted devices - comprises resistance alloy foil layer and contact elements electrically connected to each other..
DC L03 V01 V04
IN HETZLER, U
PA (ISAB-N) ISABELLENHUETTE HEUSLER GMBH KG
CYC 8
PI DE 4339551 C1 19941013 (199439)* 8p
EP 654799 A1 19950524 (199525) DE 9p
R: AT DE ES FR GB IT
JP 07192902 A 19950728 (199539) 6p
EP 654799 B1 19960918 (199642) DE 11p

R: AT DE ES FR GB IT
US 5563572 A 19961008 (199646) 7p
DE 59400691 G 19961024 (199648)
ES 2094003 T3 19970101 (199708)
US 5683566 A 19971104 (199750) 6p
ADT DE 4339551 C1 DE 1993-4339551 19931119; EP 654799 A1 EP 1994-105581 19940411; JP 07192902 A JP 1994-126824 19940516; EP 654799 B1 EP 1994-105581 19940411; US 5563572 A US 1994-247596 19940523; DE 59400691 G DE 1994-500691 19940411, EP 1994-105581 19940411; ES 2094003 T3 EP 1994-105581 19940411; US 5683566 A Div ex US 1994-247596 19940523, US 1996-649133 19960514
FDT DE 59400691 G Based on EP 654799; ES 2094003 T3 Based on EP 654799; US 5683566 A Div ex US 5563572
PRAI DE 1993-4339551 19931119
AB DE 4339551 C UPAB: 19941122
Resistance comprises a resistance layer, esp. a foil of resistance alloy, forming a path (15) and at least two contact elements (10A, 10B) made of metal electrically connected to the path (15), the elements having connecting surfaces (19) lying in a plane approx. parallel to the path (15) and with which the resistance is weldable to the connecting guide of a **circuit board**. The novelty is that plate-like contact elements (10A, 10B) are provided and are sepd. from each other by a gap (11). An insulating layer (18) is arranged on the contact elements and the resistance path (15) is arranged on the insulating layer (18). A metal layer (16) connecting the path (15) to the contact elements is arranged on the edges of the insulating layer (18). Prodn. of the resistance is also claimed.
USE - In surface mounted devices (SMDs).
Dwg.2/5

L23 ANSWER 15 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1993-145706 [18] WPIX
DNN N1993-111339
TI Device for detecting opening of an appts e.g. electric meter - includes metal washer and **resistive** and **conductive** tracks on **circuit board** to detect movement of washer.
DC S01 W05 X12
IN PLOIX, O
PA (SAGE) SAGEM SOC APPL GEN ELEC & MEC
CYC 6
PI EP 540376 A1 19930505 (199318)* FR 4p
R: BE ES FR GB IT NL
FR 2681134 A1 19930312 (199319)
ADT EP 540376 A1 EP 1992-402420 19920904; FR 2681134 A1 FR 1991-10989 19910905
PRAI FR 1991-10989 19910905
AB EP 540376 A UPAB: 19931112
The device comprises a box (1) and a cover (2) held in place by a screw (3). A washer (8) is fitted around the screw, lying in contact with a resistive track (7) and a conductive track (6) on a board (4). The two tracks allow the angular position of the washer to be detected, and this information is held in memory. A microprocessor compares the actual position of the washer with the memorised position in order to indicate any discrepancy.
USE/ADVANTAGE - Applicable for remote detection of opening of appts. Capable of signalling opening of electricity meter.
Dwg.1/2

L23 ANSWER 16 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1992-300338 [36] WPIX
DNN N1992-230005
TI Key-pad appts. for e.g. radiotelephone - includes light-pipe having two

sides and coating reflecting light inside and electrical circuit opposite keys on pad.

DC U21 V03 V04 W01
IN CHARLIER, M L
PA (MOTI) MOTOROLA INC
CYC 6
PI WO 9214345 A1 19920820 (199236)* EN 14p
W: BR CA DE GB JP
US 5153590 A 19921006 (199243) 8p
DE 4290260 T 19930128 (199305) 14p
BR 9204095 A 19930608 (199327)
GB 2263198 A 19930714 (199328) 1p
JP 05505929 W 19930826 (199339)
DE 4244815 A1 19950126 (199509) 1p
GB 2263198 B 19950524 (199524) 2p
DE 4290260 C2 19960321 (199616) 7p
DE 4244815 C1 19970410 (199719) 7p
JP 2969533 B2 19991102 (199951) 6p
ADT WO 9214345 A1 WO 1992-US505 19920121; US 5153590 A US 1991-650151 19910204; DE 4290260 T DE 1992-4290260 19920121, WO 1992-US505 19920121; BR 9204095 A BR 1992-4095 19920121, WO 1992-US505 19920121; GB 2263198 A WO 1992-US505 19920121, GB 1992-15532 19920722; JP 05505929 W JP 1992-507227 19920121, WO 1992-US505 19920121; DE 4244815 A1 DE 1992-4244815 19920121, Div ex DE 1992-4290260 19920121; GB 2263198 B WO 1992-US505 19920121, GB 1992-15532 19920722; DE 4290260 C2 DE 1992-4290260 19920121, WO 1992-US505 19920121; DE 4244815 C1 DE 1992-4244815 19920121, Div ex DE 1992-4290260 19920121; JP 2969533 B2 JP 1992-507227 19920121, WO 1992-US505 19920121
FDT DE 4290260 T Based on WO 9214345; BR 9204095 A Based on WO 9214345; GB 2263198 A Based on WO 9214345; JP 05505929 W Based on WO 9214345; DE 4244815 A1 Div ex DE 4290260; GB 2263198 B Based on WO 9214345; DE 4290260 C2 Div in DE 4244815, Based on WO 9214345; DE 4244815 C1 Div ex DE 4290260; JP 2969533 B2 Previous Publ. JP 05505929, Based on WO 9214345
PRAI US 1991-650151 19910204
AB WO 9214345 A UPAB: 19931006
The lightpipe coating is disposed upon a first side of the lightpipe and reflects light inside the lightpipe, and the electrical circuit is disposed upon the second side of the lightpipe and essentially opposite the keys on the keypad and the first side of the lightpipe.

The apparatus further includes detents moulded into the second side of the lightpipe, light reflector ramps moulded into the first side of the lightpipe and opposite to the detents. Light sources are disposed within the detents and coupled to the electrical circuit. The electrical circuit comprises **conductive** and **resistive** ink printed on the second side of the lightpipe.

ADVANTAGE - More efficient use of **circuit board** and reduced amount of wirings.

1/4

L23 ANSWER 17 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1991-090910 [13] WPIX
CR 1990-226000 [30]; 1990-323466 [43]; 1997-395794 [37]
DNN N1995-187815
TI Multilayer hybrid circuit prodn. method, with inductor, capacitor and-or resistor in PCB - involves forming passive components and in thick film process, with internal wiring layers, attaching side terminals to multilayer structure for external connections and finally sintering hybrid circuit.
DC U11 U14 V01 V02 V04
IN MOCHIZUKI, Y; TAKAYA, M
PA (DENK) TDK CORP

CYC 3
PI JP 03035586 A 19910215 (199113)* 4p
KR 9310076 B1 19931014 (199438)
US 5428885 A 19950704 (199532)B 16p
ADT JP 03035586 A JP 1989-170842 19890702; KR 9310076 B1 KR 1990-397 19900113; US 5428885 A Cont of US 1990-464453 19900112, Cont of US 1991-791896 19911113, US 1993-9410 19930127
PRAI JP 1989-170842 19890702; JP 1989-7378 19890114; JP 1989-50773 19890302

AB US 5428885 A UPAB: 19950818 ABEQ treated as Basic
The multilayer hybrid circuit mfr. involves forming a laminated body with at least dielectric layers, magnetic layers, and/or conductive patterns, so that the laminated body includes a number of passive elements with at least a capacitor layer or an inductor layer, and a resistor layer, with a semiconductor IC mounted on the laminated body. The capacitor layer is produced from dielectric layers and conductive layers in a thick film process; the inductor is produced from magnetic layers and U-shaped conductive layers, providing a coil, in a thick film process; the resistor layer is produced by attaching an insulating layer on one surface of the laminated body and then attaching a **resistive** layer and **conductive** layer on the insulation layer in a thick film process.

An internal wiring section is formed on the laminated body by laminating insulation layers and flat conductive layers, with through holes in the insulation layers to electrically couple the conductive layers on different levels of the wiring section and to couple two of the passive elements. External connection to and between the passive elements is formed by side terminals positioned on side walls of the laminated body. The laminated body is sintered at about 800deg. C. All of the steps prior to the final are performed without baking of the circuit being produced. Pref. a bare IC is attached to a conductive film, formed on one surface of the laminated body by thick film printing.

ADVANTAGE - Dense component mounting.

Dwg.4/8

AB JP 03035586 A UPAB: 19981014
The multilayer hybrid circuit mfr. involves forming a laminated body with at least dielectric layers, magnetic layers, and/or conductive patterns, so that the laminated body includes a number of passive elements with at least a capacitor layer or an inductor layer, and a resistor layer, with a semiconductor IC mounted on the laminated body. The capacitor layer is produced from dielectric layers and conductive layers in a thick film process; the inductor is produced from magnetic layers and U-shaped conductive layers, providing a coil, in a thick film process; the resistor layer is produced by attaching an insulating layer on one surface of the laminated body and then attaching a resistive layer and conductive layer on the insulation layer in a thick film process.

An internal wiring section is formed on the laminated body by laminating insulation layers and flat conductive layers, with through holes in the insulation layers to electrically couple the conductive layers to different levels in the wiring section and to couple two of the passive elements. External connection to and between the passive elements is formed by side terminals positioned on side walls of the laminated body. The laminated body is sintered at about 800 deg. C. All of the steps prior to the final are performed without baking of the circuit being produced. Pref. a bare IC is attached to a conductive film, formed on one surface of the ;aminated body by thick film printing.

ADVANTAGE - Dense component mounting. (Based on equivalent US5428885).

Dwg.0/0

L23 ANSWER 18 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1990-323466 [43] WPIX
CR 1990-226000 [30]; 1991-090910 [13]; 1997-395794 [37]
DNN N1995-187815
TI Multilayer hybrid circuit prodn. method, with inductor, capacitor and-or resistor in PCB - involves forming passive components and in thick film process, with internal wiring layers, attaching side terminals to multilayer structure for external connections and finally sintering hybrid circuit.
DC U11 U14 V01 V02 V04
IN MOCHIZUKI, Y; TAKAYA, M
PA (DENK) TDK CORP
CYC 3
PI JP 02229462 A 19900912 (199043)*
KR 9310076 B1 19931014 (199438)
US 5428885 A 19950704 (199532)B 16p
ADT JP 02229462 A JP 1989-50773 19890302; KR 9310076 B1 KR 1990-397 19900113; US 5428885 A Cont of US 1990-464453 19900112, Cont of US 1991-791896 19911113, US 1993-9410 19930127
PRAI JP 1989-50773 19890302; JP 1989-7378 19890114; JP 1989-170842 19890702
AB US 5428885 A UPAB: 19950818 ABEQ treated as Basic
The multilayer hybrid circuit mfr. involves forming a laminated body with at least dielectric layers, magnetic layers, and/or conductive patterns, so that the laminated body includes a number of passive elements with at least a capacitor layer or an inductor layer, and a resistor layer, with a semiconductor IC mounted on the laminated body. The capacitor layer is produced from dielectric layers and conductive layers in a thick film process; the inductor is produced from magnetic layers and U-shaped conductive layers, providing a coil, in a thick film process; the resistor layer is produced by attaching an insulating layer on one surface of the laminated body and then attaching a **resistive** layer and **conductive** layer on the insulation layer in a thick film process.

An internal wiring section is formed on the laminated body by laminating insulation layers and flat conductive layers, with through holes in the insulation layers to electrically couple the conductive layers on different levels of the wiring section and to couple two of the passive elements. External connection to and between the passive elements is formed by side terminals positioned on side walls of the laminated body. The laminated body is sintered at about 800deg. C. All of the steps prior to the final are performed without baking of the circuit being produced. Pref. a bare IC is attached to a conductive film, formed on one surface of the laminated body by thick film printing.

ADVANTAGE - Dense component mounting.

Dwg.4/8
AB JP 02229462 A UPAB: 19970922
Alloy wire has a space open to the side surface of the wire in axial direction in the inside of the wire material comprising shape memory alloy, the space and the opening are narrowed at low temps., and at least part of the outer periphery of the wire material is expanded toward the outside as a result of expansion of the space and the opening caused by shape recovery by heating.

Insulating substrate has electronic components with lead wire comprising the shape memory alloy wire mounted on the substrate by fitting the components on the substrate.

USE - For mounting electronic components on a substrate without soldering. @(8pp Dwg.No.6/11)@

L23 ANSWER 19 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1990-226000 [30] WPIX

CR 1990-323466 [43]; 1991-090910 [13]; 1997-395794 [37]
DNN N1995-187815
TI Multilayer hybrid circuit prodn. method, with inductor, capacitor and-or resistor in PCB - involves forming passive components and in thick film process, with internal wiring layers, attaching side terminals to multilayer structure for external connections and finally sintering hybrid circuit.
DC U11 U14 V01 V02 V04
IN MOCHFIZUKI, Y; TAKAYA, M; MOCHIZUKI, Y
PA (DENK) TDK CORP
CYC 7
PI EP 379404 A 19900725 (199030)*
R: DE FR GB NL
JP 02187054 A 19900723 (199035)
EP 379404 A3 19930331 (199350)
KR 9310076 B1 19931014 (199438)
US 5428885 A 19950704 (199532)B 16p
ADT EP 379404 A EP 1990-400092 19900112; JP 02187054 A JP 1989-7378 19890114; KR 9310076 B1 KR 1990-397 19900113; US 5428885 A Cont of US 1990-464453 19900112, Cont of US 1991-791896 19911113, US 1993-9410 19930127
PRAI JP 1989-7378 19890114; JP 1989-50773 19890302; JP 1989-170842 19890702
AB US 5428885 A UPAB: 19950818 ABEQ treated as Basic
The multilayer hybrid circuit mfr. involves forming a laminated body with at least dielectric layers, magnetic layers, and/or conductive patterns, so that the laminated body includes a number of passive elements with at least a capacitor layer or an inductor layer, and a resistor layer, with a semiconductor IC mounted on the laminated body. The capacitor layer is produced from dielectric layers and conductive layers in a thick film process; the inductor is produced from magnetic layers and U-shaped conductive layers, providing a coil, in a thick film process; the resistor layer is produced by attaching an insulating layer on one surface of the laminated body and then attaching a **resistive** layer and **conductive** layer on the insulation layer in a thick film process.

An internal wiring section is formed on the laminated body by laminating insulation layers and flat conductive layers, with through holes in the insulation layers to electrically couple the conductive layers on different levels of the wiring section and to couple two of the passive elements. External connection to and between the passive elements is formed by side terminals positioned on side walls of the laminated body. The laminated body is sintered at about 800deg. C. All of the steps prior to the final are performed without baking of the circuit being produced. Pref. a bare IC is attached to a conductive film, formed on one surface of the laminated body by thick film printing.

ADVANTAGE - Dense component mounting.

Dwg.4/8

AB EP 379404 A UPAB: 19970922
The multilayer bybrid circuit looks like a conventional printed **circuit board** and has a laminated body (1) with a number of dielectric layers magnetic layers, and conductive patterns (19) which create capacitors, inductors and resistors and mounts a semicondcutor chip (2). External connections are achieved by side terminals (11) and the whole unit can be moulded together by plastic (4) to appear as a conventional chip. Capacitors consist of a dielectric layer and conductive layers coupled to the side terminals.

Inductors are formed by sandwiching the magnetic layer between the conductive layers. Resistors are formed from adielectric layer with a resistor layer deposited on it and a condcutive layer to the side terminals.

ADVNATAGE ADVANTAGE - Provides strong package using little wiring space and reducing termianl connections. @(17pp DWg.No. 1/8)@

L23 ANSWER 20 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1983-709871 [28] WPIX
DNN N1983-121950 DNC C1983-066397
TI Binder for stencilling electroconductive paste - contains ethyl cellulose, butyl-carbitol acetate, isoamyl salicylate and stearic acid.
DC A85 L03 U11 V04 X12
IN KOSMYNIN, V V; MOGILA, N I
PA (ARTA-I) ARTAMONOV A A
CYC 1
PI SU 955215 A 19820830 (198328)* 4p
PRAI SU 1980-2996354 19801021
AB SU 955215 A UPAB: 19930925
Organic binder for **conductive** and **resistive** pastes used for stencilling printed **circuit boards** has the compsn. (in wt. %): ethyl cellulose 5.0-9.05, butyl-carbitol-acetate 59.9-62.4, isoamyl salicylate 30.0-31.2 and stearic acid 0.5-1.5. Presence of stearic acid enhances the quality of the imprint.

Typically, a binder comprises (in wt. %): ethyl cellulose 9.5, butyl-carbitol-acetate 60:30, isoamyl salicylate 30.15 and stearic acid 0.5. It is used in an amt. 15.7% to form a paste with a powder compsn. (in wt. %): Ag 70-72, Pd 20-22, Bi203 3-3.5 and glass 4.5-4. Printed lines of width 300 micron and thickness 50-70 micron have a spread of 16 micron. Bul.32/30.8.82.

L23 ANSWER 21 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1982-B6626E [07] WPIX
TI PCB on non-expansion base plate - includes elastomer film, and aqueous adhesive printing paste containing **conductive resistive** or dielectric material.
DC V04
PA (NISH-N) NIPPON SHASHIN IMSA
CYC 1
PI JP 57002595 A 19820107 (198207)* 7p
PRAI JP 1980-76125 19800605

L23 ANSWER 22 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1981-L7123D [45] WPIX
TI Pressure sensitive switch structure - includes pair of electrodes separated by resilient resistive material, sensor and amplifier and array of switches.
DC T04 U21 V03 W05
IN PEARSON, B J
PA (SPER) SPERRY CORP
CYC 1
PI US 4296406 A 19811020 (198145)* 7p
PRAI US 1979-107970 19791228
AB US 4296406 A UPAB: 19930915
Beneath a conductive foil (26) there is provided a sheet of **conductive-resistive** material. In the preferred embodiment a 4 mil thickness VELOSTAT (TM) sheet is employed in the illustrated keyboard array. Printed **circuit board** (28) is provided with etched foil conductive pads (29) aligned directly below the push-button areas (24). Each of the conductive pads (29) is provided with an individual lead (30) connected to it.

As explained before, it will be understood that the depression of any one of the push-button areas (24) with a light finger pressure causes the resistance between the ground plane (26) and the etched foil areas (29) to be reduced from a very high resistance value to a low resistance value which may be sensed on lines (30).

L23 ANSWER 23 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1979-64910B [36] WPIX
TI Aromatic polyamide imide used in electrical applications - e.g. **circuit boards** and capacitors, has high stability towards heat and moisture (NL 21.8.79).
DC A26 A85 L03 P73 U12 U14 V01 V04 X12
IN KIMURA, T; OHMURA, K; SHIBASAKI, I
PA (ASAH) ASAHI KASEI KOGYO KK
CYC 6
PI DE 2905857 A 19790830 (197936)*
NL 7901256 A 19790821 (197936)
GB 2016487 A 19790926 (197939)
JP 54110266 A 19790829 (197941)
JP 54143462 A 19791108 (197951)
JP 54153298 A 19791203 (198003)
JP 54154071 A 19791204 (198003)
JP 54154080 A 19791204 (198003)
JP 55015826 A 19800204 (198011)
JP 55015827 A 19800204 (198011)
JP 55015862 A 19800204 (198011)
JP 55016026 A 19800204 (198011)
JP 55016054 A 19800204 (198011)
JP 55016319 A 19800205 (198011)
JP 55016377 A 19800205 (198011)
JP 55018425 A 19800208 (198012)
JP 55018426 A 19800208 (198012)
DE 2953498 A 19801023 (198044)
JP 57022161 B 19820512 (198222)
JP 57022162 B 19820512 (198222)
CA 1123981 A 19820518 (198223)
JP 57026698 B 19820605 (198226)
JP 57026700 B 19820605 (198226)
GB 2016487 B 19830223 (198308)
GB 2103633 A 19830302 (198309)
GB 2104084 A 19830322 (198314)
US 4377652 A 19830315 (198315)
CA 1143084 A 19830622 (198325)
GB 2104084 B 19830713 (198328)
GB 2103633 B 19850716 (198532)
JP 60030353 B 19850829 (198539)
JP 60038011 B 19851211 (198602)
JP 60056622 B 19860925 (198639)
DE 2905857 C 19861218 (198703)
JP 61059906 B 19870518 (198724)
NL 181739 B 19880428 (198821)
JP 63020707 B 19890629 (198926)
DE 2953498 C
PRAI JP 1978-90934 19780727; JP 1978-16612 19780217; JP 1978-51214 19780428; JP 1978-61637 19780525; JP 1978-62604 19780525; JP 1978-62605 19780525; JP 1978-88363 19780721; JP 1978-88364 19780721; JP 1978-88365 19780721; JP 1978-88367 19780721; JP 1978-89391 19780724; JP 1978-89392 19780724; JP 1978-89393 19780724; JP 1978-90933 19780727
AB DE 2905857 A UPAB: 19930901
Article for electrical applications consists (partly) of an aromatic polyamideimied (I) with a reduced viscosity of 0.3-1.5, pref. 0.4-1.3 and recurring units of the formulae =(N-Ar-NH-R)= --(NH-circle with diagonal line'-NH-T=N-Ar' or Ar"-N=T)- -(NH-Ar or Ar'-NH-T=N-circle with diagonal line'-circle with diagonal line'-N-T)-, -(NH-circle with diagonal line'-NH-T=N-Ar' or Ar"'N=R)- or -(NH-Ar" or

Ar'-NH-T=N-circle with diagonal line'-N=T)- in which -T is derived from trimellitic acid and has the formula Ar is -circle with diagonal"-, -circle with diagonal line"-circle with diagonal line"-circle with diagonal line"-, -circle with diagonal line"-X-circle with diagonal line- or -circle with diagonal line'-X-circle with diagonal line-X-circle with diagonal line-X-circle with diagonal line', Ar' is -circle with diagonal line"'-, -circle with diagonal line"'-circle with diagonal line"'- or -circle with diagonal line"'-X-circle with diagonal line"'. Ar" is -circle with diagonal line"-, -circle with diagonal line"-X-circle with diagonal line"- or circle with diagonal line'-X-circle with diagonal line-X-circle with diagonal line-X-circle diagonal line'. Ar"' is -0"-X-0"- or -circle with diagonal line'-X-circle with diagonal line-X-circle with diagonal line-x-circle with diagonal line'-. circle with diagonal line is phenylene. circle with diagonal line' is m-phenylene. circle with diagonal line" is m-phenylene with an R substit., R being H, halogen or 1-4C alkyl. circle with diagonal line"' is p-phenylene with an R substit. X is O, S, SO2, CO, COO, CH, CH2CH2, or Cme2).

(I) and compsns. contg. (I) are specified for impregnating (laminated) paper or fibres used for printed circuits and hybrid circuits and for capacitors. (I) has excellent thermal stability, resistance to moisture, storage stability and electrical properties. It can be made **conductive**, **resistive**, dielectric or insulating and these properties are accurate and reliable.

L23 ANSWER 24 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1979-59174B [32] WPIX
TI Thick-film multilayer printed **circuit board** prodn. - using glass frit as binder in both the insulating and the **conductive** or **resistive** layers.
DC L03 U12 U14 V04
PA (HITA) HITACHI LTD
CYC 1
PI JP 54019050 B 19790712 (197932)*
JP 50065869 A 19750603 (197932)
PRAI JP 1973-115824 19731017
AB JP 79019050 B UPAB: 19930901
Insulating layers and **conductive** or **resistive** layers are formed on an insulating substrate by coating the substrate with paste and firing it. The paste for the insulating layers and the paste for the **conductive** or **resistive** layers contains, as a binder, glass frit having the same compsn.

L23 ANSWER 25 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1976-L1404X [46] WPIX
TI Power controller for electrical loads - has bridging contact slidingly engaging **conductive** and **resistive** tracks on **circuit board**.
DC V01
PA (INPO-N) IND POWER CONTROLS INC
CYC 1
PI US 3990033 A 19761102 (197646)*
PRAI US 1975-579255 19750520; US 1976-647640 19760108; US 1977-797528 19770516
AB US 3990033 A UPAB: 19930901
The components of the controller are protectively enclosed in a rectangular enclosure or housing (12) made of an electrically insulating material. The housing has an open end closed by a standard type of switch mounting strap (14) to which the housing is secured. The mounting strap with the housing projecting rearwardly from it is therefore adapted to be installed behind a standard switch wall plate, with the housing (12)

received within a standard wall mounted switch of power receptacle box. The mounting strap (14) is accordingly provided with mounting slots (16) and a central slot receiving a centering insert and slot closure (18) through which a manual control lever arm (20) projects.

L23 ANSWER 26 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1975-28876W [17] WPIX
TI Selective etchant for nickel and alloys in presence of copper - for use in **circuit board** manufacture.
DC L03 M14
PA (MICA-N) MICA CORP
CYC 1
PI US 3878006 A 19750415 (197517)*
PRAI US 1973-410226 19731026
AB US 3878006 A UPAB: 19930831
An etching composition for the selective removal of Ni or Ni alloy in the presence of Cu comprises 0.5-1.5 M CuSO4 SH2O, pref. 250 g/l and 0.02-2.0 M conc. H2SO4 pref. 2 ml/l. Printed **circuit board** stock consisting of an insulating support at least one layer of Ni or Ni alloy resistance material adhering thereto and a layer of highly conductive Cu adhering to the resistance material is etched using a resist to form a pattern of **conductive** and **resistive** areas and any unwanted resistor layer is then etched using the etchant, preferably at 130 degrees - 200 degrees F. Ni-P alloy resistive layers may be removed from between Cu lines on a printed **circuit board** without deleterious effect.

L23 ANSWER 27 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1973-76910U [50] WPIX
TI **Circuit board** - by selective removal of **conductive** and **resistive** layers then semiconductor fixing by heating and rubbing.
DC L03 U11
PA (OLIT) OLIVETTI & CO SPA
CYC 1
PI US 3775838 A (197350)*
PRAI US 1971-120185 19710302; US 1972-246595 19720424
AB US 3775838 A UPAB: 19930831
A semiconductor-carrying **circuit board** is prepared by successively forming evaporated **resistive** and first **conductive** layers on an insulating substrate, electroplating a second conductive layer on a region of the first, removing from a second different region both evaporated layers, removing from a third different region the first conductive layer, thereby forming conductors, insulators and resistors on the board, and affixing semiconductor elements to the conductors by heating with hot gas and scrubbing them on the conductors to form a eutectic.

L23 ANSWER 28 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1972-62046T [39] WPIX
TI Printed **circuit board** stock - plating **resistive** on **conductive** layer through porous membrane gives uniform resistance.
DC A14 A85 L03
PA (MICA-N) MICA CORP
CYC 1
PI US 3691007 A (197239)*
PRAI US 1969-850248 19690814
AB US 3691007 A UPAB: 19930831
Printed **circuit board** stock is for completion by etching technique into boards having patterns of conductors and resistors

in adjacent layers. The stock is made by coating a conductive foil with a porous membrane, and plating an electrically resistive layer on to the foil through the membrance which is then removed. A substrate is laminated to the resistive side. Pref. the foil is Cu and the plated layer Ni or Ni phosphorous. The membrane is formed by a dip in polyvinylidene fluoride 1% dimethylformamide sol., or in cellulose triacetate 0.1% trichlorethane soln. Resistance across the width of 5" x 8" stock is held to within plus-or-minus 10% and all the resistors can be produced to close tolerances with high uniformity from board to board.

L23 ANSWER 29 OF 29 WPIX (C) 2003 THOMSON DERWENT
AN 1971-01788S [01] WPIX
TI Yig composition for solid state transformer.
DC L03
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 3553433 A (197101)*
PRAI US 1964-367462 19640514; US 1964-398480 19640918; US 1968-720009 19680202
AB US 3553433 A UPAB: 19930831
Yttrium iron garnet of formula MxY(3-x)AqFe(5-q)O12 where M and A are each one of Al, Ga, In, Th, La, Sc or a rare earth element: x is 0-3; q 0-5; x and q being integers and x being <3 when q = 5 and q being <5 when X = 3. The YIG has a comparatively conductive zone integral with and autogenously formed by reduction of part only of the YIG. The YIG is esp. a **circuit board** substrate with **conductive** and **resistive** portion formed by the reduction process taken to various stages to form a solid state transformer circuit.

L25 ANSWER 1 OF 1 WPIX (C) 2003 THOMSON DERWENT
AN 1997-145051 [13] WPIX
DNN N1997-120077
TI Electronic power converter circuit using low temp. co-fired ceramic substrates for frequencies not exceeding 30 MHz - uses favourable characteristics and features of LTCC substrates to maximise number of active components which can be formed internal to substrate.
DC U11 U14
IN MCCLANAHAN, R F; SHAPIRO, A A; WASHBURN, R D
PA (HUGA) HUGHES ELECTRONICS
CYC 1
PI US 5604673 A 19970218 (199713)* 10p
ADT US 5604673 A US 1995-479293 19950607
PRAI US 1995-479293 19950607
AB US 5604673 A UPAB: 19970326
The circuit includes a low temp. co-fired ceramic substrate layers and an electronic power converter circuit having selected **passive components** chosen from capacitors, resistors, inductors, and transformers and formed as an integral part of one or more of the layers of the low-temp. co-fired ceramic substrate.

At least one conductive layer located on or within the low temp. co-fired ceramic substrate, electrically connects the circuitry of the electronic power converter circuit.

ADVANTAGE - Use of such substrate allows selection of various **conductive** and **resistive** links to precisely form interconnection circuitry and selected non-semiconductor components which improves stability and reduce cost of power conversion circuits.
Dwg.3/5

L29 ANSWER 1 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 2002-179319 [23] WPIX
DNN N2002-136421 DNC C2002-055547
TI Electronic device used as, e.g. varistor, includes multi-sided body and terminals coated with polymer which is resistant to plating of metal onto the exterior surface of body.
DC A32 A85 L03 U11 V01
IN **GALVAGNI, J L**; HEISTAND, R H; KENNEDY, R M; MEVISSEN, J P
PA (AVXA-N) AVX CORP; (GALV-I) GALVAGNI J L; (HEIS-I) HEISTAND R H; (KENN-I) KENNEDY R M; (MEVI-I) MEVISSEN J P
CYC 94
PI WO 2001075940 A2 20011011 (200223)* EN 28p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
AU 2001047707 A 20011015 (200223)
US 2001035810 A1 20011101 (200223)
ADT WO 2001075940 A2 WO 2001-US9299 20010323; AU 2001047707 A AU 2001-47707 20010323; US 2001035810 A1 Provisional US 2000-193276P 20000330, US 2001-810829 20010316
FDT AU 2001047707 A Based on WO 200175940
PRAI US 2001-810829 20010316; US 2000-193276P 20000330
AB WO 200175940 A UPAB: 20020411
NOVELTY - Electronic device includes a multi-sided body defined by electrode plates, and terminals electrically connected to the electrode plates. The multi-sided body and the terminals are capable of receiving a polymer coating. The polymer coating is resistant to plating of metal onto the exterior surface of the body.

DETAILED DESCRIPTION - An electronic device includes a multi-sided body defined by electrode plates arranged in a stack, and terminals electrically connected to the electrode plates in a predetermined manner and having layers on their exterior surface. The multi-sided body and the terminals are capable of receiving a polymer coating. The multi-sided body has a polymer coating on at least a portion of its exterior surface. The polymer coating is resistant to plating of metal onto the exterior surface of the body. The terminals comprise metal plating layer(s) on their exterior surface. A metal plating is fixed to a polymer coating on the terminals.

An INDEPENDENT CLAIM is also included for a process of making an electronic device involving providing a multi-sided body having on its interior stacked electrode plates, providing terminals connected to the electrode plates, coating the electronic device on all sides with a thermoset resin, curing the resin, and plating the metal upon the terminals.

USE - As varistor (preferably), thermistor, or resistor or other semiconductor devices (claimed).

ADVANTAGE - The invention prevents undesirable plating upon the main body of the microelectronic device, while still facilitating plating upon the end terminations. Selective removal of resin, which is difficult and costly in the manufacture of electronic devices of very small size, can be avoided.
Dwg.0/3

L29 ANSWER 2 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1999-153337 [13] WPIX
DNN N1999-110566
TI Multilayer ceramic RC device - has two ceramic layers, one on top of

other, where each layer has circuitry on it with series resistance and capacitor electrode of respective polarity, with electrodes on capacitor body and connected to circuitry.

DC U25 V01
IN **GALVAGNI, J L**; RITTER, A P
PA (AVXA-N) AVX CORP
CYC 83
PI WO 9905786 A1 19990204 (199913)* EN 43p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
US 5889445 A 19990330 (199920)
AU 9875717 A 19990216 (199926)
EP 998784 A1 20000510 (200027) EN
R: BE CH DE DK FI FR GB IE IT LI NL SE
CN 1265238 A 20000830 (200059)
JP 2001511607 W 20010814 (200154) 33p
KR 2001022155 A 20010315 (200159)
ADT WO 9905786 A1 WO 1998-US9816 19980514; US 5889445 A US 1997-898695 19970722; AU 9875717 A AU 1998-75717 19980514; EP 998784 A1 EP 1998-923418 19980514, WO 1998-US9816 19980514; CN 1265238 A CN 1998-807530 19980514; JP 2001511607 W WO 1998-US9816 19980514, JP 2000-504656 19980514; KR 2001022155 A KR 2000-700726 20000122
FDT AU 9875717 A Based on WO 9905786; EP 998784 A1 Based on WO 9905786; JP 2001511607 W Based on WO 9905786
PRAI US 1997-898695 19970722
AB WO 9905786 A UPAB: 19990331
NOVELTY - The multilayer ceramic RC device (10) has two ceramic layers (32), one on top of the other. Each layer has circuitry on it with a series resistance (34,36) and a capacitor electrode (28,30) of respective polarity. The electrodes are positioned on a capacitor body and are connected to the circuitry.
USE - None given.
ADVANTAGE - Uses embedded resistors which reduces space taken up by device. DESCRIPTION OF DRAWING(S) - The drawing shows a cross sectional view of a multilayer ceramic RC device.
Dwg.1A/7

L29 ANSWER 3 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1999-095993 [08] WPIX
DNN N1999-069763
TI Surface mount multi-layer ceramic capacitor for printed circuit board - has interleaved electrodes plates with interdigitated lead structures providing multiple, adjacent current injection points onto associated main electrode portion.
DC V01 V04
IN DUPRE, D A; **GALVAGNI, J L**; RITTER, A P; DUPRE', D A
PA (AVXA-N) AVX CORP
CYC 83
PI WO 9900807 A1 19990107 (199908)* EN 34p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
US 5880925 A 19990309 (199917)
AU 9873871 A 19990119 (199922)

EP 995207 A1 20000426 (200025) EN
R: BE CH DE DK ES FI FR GB IE IT LI NL SE
CN 1261457 A 20000726 (200057)
US 6243253 B1 20010605 (200133)
KR 2001020511 A 20010315 (200159)
JP 2002508114 W 20020312 (200220) 27p
ADT WO 9900807 A1 WO 1998-US9873 19980514; US 5880925 A US 1997-884597 19970627; AU 9873871 A AU 1998-73871 19980514; EP 995207 A1 EP 1998-921208 19980514, WO 1998-US9873 19980514; CN 1261457 A CN 1998-806558 19980514; US 6243253 B1 Cont of US 1997-884597 19970627, US 1999-264124 19990308; KR 2001020511 A KR 1999-712280 19991224; JP 2002508114 W WO 1998-US9873 19980514, JP 1999-505532 19980514
FDT AU 9873871 A Based on WO 9900807; EP 995207 A1 Based on WO 9900807; US 6243253 B1 Cont of US 5880925; JP 2002508114 W Based on WO 9900807
PRAI US 1997-884597 19970627; US 1999-264124 19990308
AB WO 9900807 A UPAB: 19990224
The capacitor comprises a low-aspect capacitor body including first and second electrode plates (58,60) interleaved in opposed and spaced apart relation. Layers of dielectric material to provide a predetermined dielectric constant separate the electrode plates. Each of the first and second electrode plates includes a main electrode portion (64,68) and spaced apart lead structures (66,70) extending from it, respective lead structures of the first electrode plates being located adjacent respective lead structures of the second electrode plates in an interdigitated arrangement. Corresponding lead structures of respective first electrode plates are electrically connected together and corresponding lead structures of respective second electrodes plates are electrically connected together to define electrical terminals of a first polarity and electrical terminals of a second polarity, respectively. Preferably, the electrical terminals are formed by a thick-film terminal material.
ADVANTAGE - Low inductance. Offset nature of lead structure on opposite lateral sides of each electrode plate also reduces mutual inductance levels.
Dwg.6/11

L29 ANSWER 4 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1998-494058 [42] WPIX
CR 1996-251284 [25]
DNN N1998-385803
TI Decoupling capacitor manufacturing method for computer system - involves arranging two dielectrics with barrier inbetween, having decoupling characteristic at mutually different temperature between two electrode plates.
DC V01
IN **GALVAGNI, J**; MURPHY, R G; SAXENMEYER, G J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5799379 A 19980901 (199842)* 7p
ADT US 5799379 A Cont of US 1992-978794 19921119, Div ex US 1994-277791 19940720, US 1995-446247 19950522
FDT US 5799379 A Div ex US 5517385
PRAI US 1992-978794 19921119; US 1994-277791 19940720; US 1995-446247 19950522
AB US 5799379 A UPAB: 19981021
The method involves calculating total capacitance value and area of two electrode plates (11,13). Then desired thickness of two dielectrics (1,2) are calculated. The material composition of both the dielectrics are different. The temperature at which dielectrics provide decoupling also differ mutually.
The two dielectrics are separated by a barrier (17) and are placed inbetween the two electrode plates and contact them electrically. The

barrier prevents intermingling of the two dielectrics.
ADVANTAGE - Maintains decoupling effectiveness over wide range of operating temperature.
Dwg.1/8

L29 ANSWER 5 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1997-332017 [30] WPIX
DNN N1997-275623 DNC C1997-106500
TI Making a planar ceramic multilayer capacitor - by forming the capacitor as a parallelepiped with internal electrodes parallel to the base and exposed alternately at opposite ends.
DC L03 P42 V01
IN **GALVAGNI**, J
PA (AVXA-N) AVX CORP
CYC 1
PI US 5639507 A 19970617 (199730)* 6p
ADT US 5639507 A US 1995-433172 19950503
PRAI US 1995-433172 19950503
AB US 5639507 A UPAB: 19970723
A method of manufacturing a terminated ceramic capacitor comprises forming the capacitor as a parallelepiped with acute and obtuse angles between end surfaces and base. Internal electrodes are parallel to the base and exposed alternately at opposite ends. A metallic coating is formed over end faces and bases only (32) and then removed in registry with the junction portions. Also claimed is a method as above using a green ceramic matrix (12) with intervening parallel electrode layers (13) and severing the matrix to define many multiplex capacitor preforms as above which are sintered to form capacitors and the coating applied and removed as above.
USE - As miniaturised leadless ceramic capacitors for electronic equipment
ADVANTAGE - Termination is simplified and there is no need for precision masking or re-masking. The capacitance is adjustable.
Dwg.2/8

L29 ANSWER 6 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1996-496988 [49] WPIX
DNN N1996-419146
TI Tomb-stoning resistant surface mount electronic component - has outermost parts of coating overlying end surfaces with coating of non-solder wettable conductive metal.
DC U11
IN **GALVAGNI**, J; RANDALL, S P E
PA (AVXA-N) AVX CORP
CYC 1
PI US 5569880 A 19961029 (199649)* 5p
ADT US 5569880 A US 1994-348293 19941202
PRAI US 1994-348293 19941202
AB US 5569880 A UPAB: 19961205
The component includes top and bottom surfaces, side surfaces and parallel end surfaces, conductive termination device exiting at the end surfaces and a conductive termination coating overlying the end surfaces and abutting parts of at least one of the top and bottom surfaces.
The parts of the termination coating overlies the top and bottom surfaces defining spaced terminal pads formed of a metal wettable by solder. The outermost parts of the coating overlies the end surfaces with a further coating of a non-solder wettable conductive metal.
ADVANTAGE - Enables more efficient use of geography of PC board surface.
Dwg.3/3

L29 ANSWER 7 OF 17 WPIX (C) 2003 THOMSON DERWENT

AN 1996-251284 [25] WPIX
CR 1998-494058 [42]
DNN N1996-211216
TI Decoupling capacitor structure to operate at two different and spaced apart temps. - uses two different dielectrics connected between capacitor plates and sepd. by electrical insulation, providing different capacitances at different temps...
DC V01
IN **GALVAGNI**, J; MURPHY, R G; SAXENMEYER, G J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5517385 A 19960514 (199625)* 7p
ADT US 5517385 A Cont of US 1992-978794 19921119, US 1994-277791 19940720
PRAI US 1992-978794 19921119; US 1994-277791 19940720
AB US 5517385 A UPAB: 19981021
The capacitor has two plates spaced a predetermined distance apart with two different dielectric materials placed in between and in contact with both plates, providing two different capacitance values at two different temps.. One or both of the dielectric materials is divided into multiple blocks in a predetermined arrangement between said two capacitor plate means.

The dielectric materials are sepd. electrically by a low modulus material as a barrier to prevent an intermingling of the dielectrics, which can create a third dielectric material having an unknown dielectric constant.

ADVANTAGE - Small in size and functions over a wide range of operating temps., maintaining decoupling effectiveness.
Dwg.1/8

L29 ANSWER 8 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1995-106413 [14] WPIX
DNN N1995-084204
TI Solid state capacitor mfg. method - folding solid state forming metal into U-shaped trough, introducing layer of metal powder into trough, sintering powder for bonding to foil, and severing foil to form capacitors.
DC V01
IN BROWN, S; CHRISTIAN, K; **GALVAGNI**, J; QUI, Y
PA (AVXA-N) AVX CORP
CYC 1
PI US 5394295 A 19950228 (199514)* 7p
ADT US 5394295 A US 1993-68150 19930528
PRAI US 1993-68150 19930528
AB US 5394295 A UPAB: 19950412
A method of manufacturing solid state capacitors involves providing an elongate band of solid state forming metal, folding the band into a trough-like U-shaped configuration, and introducing a layer of solid state metal powder into the trough. The powdered metal is sintered to bond the metal to the foil which is then partially severed to define a multiplicity of individual units.

The units are then processed to convert the units into capacitors by sequential dielectric forming and counter-electrode depositing steps. The individual capacitors are terminated and preferably also may be tested while still interconnected by portions of the foil.

USE/ADVANTAGE- Capacitor exhibits high volumetric efficiency and is particularly adapted for surface mounting. Individual capacitor preforms are continuously linked during entire sequence of processing steps.
Dwg.1/2

L29 ANSWER 9 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1995-089458 [12] WPIX
DNN N1995-070730

TI Trapezoid chip ceramic capacitor - is formed on isosceles trapezoid in longitudinal section, e.g. termination is effected by placing larger base on support surface and stacking number of trapezoidal capacitors in side-to-side relationship.
DC V01
IN **GALVAGNI, J**
PA (AVXA-N) AVX CORP
CYC 1
PI US 5388024 A 19950207 (199512)* 6p
ADT US 5388024 A US 1993-100375 19930802
PRAI US 1993-100375 19930802
AB US 5388024 A UPAB: 19950328
The capacitor assembly includes a number of discrete radially separable interconnected ceramic capacitors arranged in a stack. Each of the capacitors has mutually spaced first and second opposite polarity terminals. The latter in one of capacitors in the stack are disposed in abutting relation to the terminals of adjacent capacitors.

Continuous first and surface conductive readily fractured termination films couple respective first and second termination of the capacitors in the stack. Hence individual capacitors or capacitors gp of mechanically and electrically connected capacitors as sub-unit may be separated from the stack.

USE/ADVANTAGE - As multiple capacitors stack for soldering on personal computer board. Minimised possibility of soldering connection will short circuit other elements on board with improved use of generator board, and easier termination.
Dwg.1-3/7

L29 ANSWER 10 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1993-126325 [15] WPIX
DNN N1993-096442
TI Surface mount solid state tantalum capacitor mfg. method - forming tantalum powder into coherent porous mass connected to container which forms anode, and forming counter electrode on dielectric.
DC V01
IN **GALVAGNI, J**
PA (AVXA-N) AVX CORP
CYC 5
PI US 5198968 A 19930330 (199315)* 8p
GB 2269051 A 19940126 (199402) 18p
DE 4319552 A1 19940127 (199405) 9p
FR 2694124 A1 19940128 (199408)
JP 06097010 A 19940408 (199419) 7p
GB 2269051 B 19961127 (199651) 1p
ADT US 5198968 A US 1992-917848 19920723; GB 2269051 A GB 1993-9582 19930510; DE 4319552 A1 DE 1993-4319552 19930612; FR 2694124 A1 FR 1993-6048 19930519; JP 06097010 A JP 1993-130657 19930601; GB 2269051 B GB 1993-9582 19930510
PRAI US 1992-917848 19920723
AB US 5198968 A UPAB: 19930924
The method involves providing a tubular tantalum container which is filled with tantalum powder. The filled tantalum container is then sintered to form the powder into a coherent porous mass which is electrically and mechanically connected to the tantalum container which forms the anode of the capacitor. The container is of tubular configuration at least one wall of which is flat and is formed (either before or after sintering) with an opening. The porous tantalum mass is subjected to processing steps including anodising to form a tantalum pentoxide dielectric layer.The dielectric coating is formed with a counter electrode by impregnation with manganous nitrate followed by heating in a moist environment to convert the manganous nitrate to manganese dioxide. ADVANTAGE - High capacitance

per volume, high shock resistance, low ESR.
1e/4

L29 ANSWER 11 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1992-007036 [01] WPIX
DNN N1992-005428
TI Delamination resistant ceramic capacitor - has augmented bonds formed between metallic electrode layers and ceramic dielectric layers and compatible intervening layers.
DC V01
IN **GALVAGNI, J**
PA (AVXA-N) AVX CORP
CYC 1
PI US 5072329 A 19911210 (199201)*
ADT US 5072329 A US 1991-678444 19910401
PRAI US 1991-678444 19910401
AB US 5072329 A UPAB: 19931006
A multilayer ceramic capacitive device resistant to delamination has intervening layers interposed between the metallic electrode layers and the dielectric layers. The intervening layers are comprised of ceramic compatible with the ceramic of the dielectric and increments of metal compatible with the electrode layers.

In the sintering process augmented bonds are formed between the electrode metal and components of metal in the intervening layers and similarly such bonds are formed between the ceramic components of the intervening layers and the dielectric components.

USE/ADVANTAGE - Delamination resistance, augmented mechanical adhesion of terminations to end faces of capacitor and improved heat dissipation. Capacitors, varistors, ceramic actuators.
1/3

L29 ANSWER 12 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1990-107582 [14] WPIX
DNN N1990-083296
TI Electrostrictive actuator or capacitor - with electrodes of opposite polarity exposed at opposite surfaces of stack of green ceramic sheets.
DC V01 V06
IN **GALVAGNI, J**
PA (AVXA-N) AVX CORP
CYC 7
PI US 4903166 A 19900220 (199014)* 6p
GB 2232532 A 19901212 (199050)
DE 3940619 A 19901213 (199051)
FR 2648288 A 19901214 (199106)
JP 03011980 A 19910121 (199109)
CA 2001435 A 19901209 (199110)
CA 2001435 C 19930921 (199344)
GB 2232532 B 19940316 (199409)
ADT US 4903166 A US 1989-363770 19890609; GB 2232532 A GB 1989-24636 19891101; DE 3940619 A DE 1989-3940619 19891208; JP 03011980 A JP 1989-323687 19891213; CA 2001435 C CA 1989-2001435 19891025; GB 2232532 B GB 1989-24636 19891101
PRAI US 1989-363770 19890609
AB US 4903166 A UPAB: 19930928
Equal size green ceramic sheets are provided, covered with a coating comprising discreet areas of electrode forming abnd pseudo electrode ink. The electrode ink areas extend to at least a first margin of the sheets and the pseudo electrode ink areas extends to at least a second margin of said sheets. A stack of a number of the sheets are formed such that the first margins of alternate layers are exposed at a first surface of the stack and the first margins of the layers intervening between the

alternate layers are exposed at a second surface of the stack.
The second margins are interposed at the surfaces between the first margins, then heating and sintering the stack, before applying conductive terminations to the first and second surfaces. The pseudo ink comprises materials subject to volitilisation responsive to the heating step to provide void areas between the layers in the areas formerly occupied by the pseudo ink areas.
USE - E.g. in printed heads of impact printer, force generating elements of relays and deflecting and forming optical surfaces.
4/4

L29 ANSWER 13 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1989-323932 [44] WPIX
DNN N1989-246719
TI Ceramic capacitor thin film termination forming method - effects final polishing of tab exposed surface using miniature abrasives and forms layers via vacuum deposition.
DC P61 V01
IN **GALVAGNI**, J; HUMENIK, J N; OBERSCHMIDT, J M; OBERSCHMID, J M
PA (AVXA-N) AVX CORP; (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP; (AUXA-N) AUX CORP
CYC 7
PI US 4862318 A 19890829 (198944)* 10p
GB 2230140 A 19901010 (199041)
DE 3936579 A 19901011 (199042)
FR 2645337 A 19901005 (199047)
JP 02288213 A 19901128 (199103)
IT 1237776 B 19930617 (199347)
GB 2230140 B 19940427 (199414)
ADT US 4862318 A US 1989-332993 19890404; GB 2230140 A GB 1989-21195 19890919; DE 3936579 A DE 1989-3936579 19891103; IT 1237776 B IT 1989-22405 19891116; GB 2230140 B GB 1989-21195 19890919
PRAI US 1989-332993 19890404
AB US 4862318 A UPAB: 19930923
The tab type ceramic capacitor shorting bar forming method includes the step of effecting a final polishing of the tab exposed surface utilising grit or abrasives of a critical size, namely of average particle size in the range of about 2 to about 10 microns. The method further employs thin film metallurgy namely the vacuum deposition or sputtering of one or more layers within specified thickness ranges.
ADVANTAGE - Uses conventional BLM technology.
4/5

L29 ANSWER 14 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1989-172596 [23] WPIX
DNN N1989-131749 DNC C1989-076370
TI Forming encapsulated metallic conductors - using mask with middle neck portion to deposit vacuum evaporated layer and broader sputtered layer.
DC L03 M13 Q71 U11 V01 X26
IN **GALVAGNI**, J; MILLER, R; MILLER, R A
PA (AVXA-N) AVX CORP; (IBMC) IBM CORP; (AUXA-N) AUX CORP; (IBMC) IMB CORP
CYC 11
PI US 4830723 A 19890516 (198923)* 5p
GB 2220108 A 19891228 (199001)
DE 3906018 A 19891228 (199002)
ES 2010414 A 19891101 (199004)
NL 8900367 A 19900116 (199006)
FR 2633453 A 19891229 (199007)
JP 01321612 A 19891227 (199007)
SE 8900611 A 19891223 (199007)
BR 8901600 A 19900410 (199019)

CH 678378 A 19910830 (199138)
IT 1229172 B 19910722 (199232)
SE 467811 B 19920914 (199240)
GB 2220108 B 19921209 (199250)
ADT US 4830723 A US 1988-209588 19880622; GB 2220108 A GB 1989-2168 19890201; DE 3906018 A DE 1989-3906018 19890227; ES 2010414 A ES 1989-636 19890222; NL 8900367 A NL 1989-367 19890215; FR 2633453 A FR 1989-1552 19890207; JP 01321612 A JP 1989-40145 19890220; IT 1229172 B IT 1989-20087 19890410; SE 467811 B SE 1989-611 19890222; GB 2220108 B GB 1989-2168 19890201
PRAI US 1988-209588 19880622
AB US 4830723 A UPAB: 19930923
Superposed or encapsulated metallic conductive paths are formed on a dielectric substrate by using a pattern mask which has wider openings at its lower surface and a contricted neck portion between its upper and lower surfaces.

A first metal pattern is deposited through the mask by vacuum evapn. to fbrm a pattern conforming to the dimension of the constricted neck portion, and a second pattern is then sputtered which will conform to the dimension of the wider lower opening and so cover and encapsulate the first pattern.

USE - In electronics devices etc. Encapsulated conductive path is formed using only one mask.
1-5/5

L29 ANSWER 15 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1987-021686 [03] WPIX
DNN N1987-016377
TI Testing method for electronic components - being for gang burning in of capacitors and using two matrices with complementing apertures filled with fuses.
DC S01 V01 V04
IN **GALVAGNI**, J; HOPKINS, L; RITCHIE, K
PA (AVXA-N) AVX CORP
CYC 1
PI US 4633175 A 19861230 (198703)* 5p
ADT US 4633175 A US 1984-674519 19841123
PRAI US 1984-674519 19841123
AB US 4633175 A UPAB: 19930922
The method comprises the steps of providing two stretchable elastomeric insulating matrices each having throughgoing apertures. The electronic devices are introduced into the apertures of the first matrix so that the devices are frictionally supported in the apertures and opposed terminals of the devices are exposed at opposite surfaces of the matrix. Replaceable fuse members are introduced into the apertures of the second matrix so that the fuse members are frictionally supported in the apertures and opposite terminals of the fuse members are exposed at opposite surfaces of the second matrix.

The two matrices are superposed so that each terminal of a fuse in the second matrix engages against a respective terminal of a device in the first matrix. The superposed matrices are interposed between two yieldable electrodes, one electrode being in conductive contact with a terminal of each of the devices and the other electrode being in conductive contact with a terminal of each of the fuses. The devices are subjected to testing conditions while simultaneously causing a voltage to be applied across the electrodes.

USE/ADVANTAGE - Simultaneous processing of ceramic capacitors. Allows proper 'burning-in' even if short circuits occur.
1/4

L29 ANSWER 16 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1980-F0208C [23] WPIX

TI Monolithic capacitor mfg. method - by exerting pressure perpendicular to electrode stack to form indentations in bottom section.
DC V01
IN **GALVAGNI, J L**
PA (AVXA-N) AVX CORP
CYC 5
PI DE 2942704 A 19800529 (198023)*
GB 2034521 A 19800604 (198023)
FR 2441912 A 19800718 (198036)
US 4297773 A 19811103 (198147)
CA 1145423 A 19830426 (198320)
GB 2034521 B 19830727 (198330)
PRAI US 1978-961247 19781116; US 1980-132083 19800320
AB DE 2942704 A UPAB: 19930902
The monolithic capacitor is fabricated in the following stages. The electrodes are assembled and fitted to a moist ceramic body in a partly overlapping arrangement. Pressure is exerted on this partial assembly in a vertical direction to the arrangement of electrodes so that indentations are formed in the bottom which extend to the edge parts.

A part of the bottom surface is at a level lying below the level of the indentations. The ceramic mass is then fired and a conducting coating applied to the edge ends. A mould is used for producing the indentations.

L29 ANSWER 17 OF 17 WPIX (C) 2003 THOMSON DERWENT
AN 1978-49428A [27] WPIX
TI Solid electrolyte chip capacitor encapsulation - in a tubular case which is cut to form anode and cathode terminals.
DC A85 L03 V01 X12
IN **GALVAGNI, J L**
PA (AVXA-N) AVX CORP
CYC 4
PI US 4085435 A 19780418 (197827)*
GB 1523249 A 19780831 (197835)
CA 1082321 A 19800722 (198032)
DE 2725137 C 19840906 (198437)
PRAI US 1976-695596 19760614
AB US 4085435 A UPAB: 19930901
Solid electrolyte chip capacitor having an outer cathode end portion, an anode body extending axially from the cathode end portion and an anode lead extending axially from the anode body, is encapsulated in a hardened mass of polymeric insulating material within an metallic case formed by axially spaced sleeves which completely enclose the cathode end portion and the anode body of the capacity. The sleeve members are connected internally respectively to the cathode end and the anode lead, and the polymeric insulating material holds the sleeve members in axially spaced alignment.

Used in prodn. of Ta chip capacitors. The method provides a capacitor which is sufficiently rugged to permit manual or automatic handling without special precautions and is highly resistant to the ingress of moisture.

L38 ANSWER 1 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 2002-529221 [56] WPIX
DNN N2002-419132
TI **Electric circuit** module has voltage-controlled switch with **passive components** forming low pass filter in multilayer ceramic passive module; switch is on base body upper or lower side.
DC U21 U25
IN BLOCK, C; FLUEHR, H
PA (EPCO-N) EPCOS AG
CYC 22
PI WO 2002058239 A2 20020725 (200256)* DE 20p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: CN JP US
DE 10102201 A1 20020829 (200264)
ADT WO 2002058239 A2 WO 2002-DE129 20020117; DE 10102201 A1 DE 2001-10102201 20010118
PRAI DE 2001-10102201 20010118
AB WO 200258239 A UPAB: 20021031
NOVELTY - The module has a voltage-controlled switch with transmitter and receiver inputs and an output and selectively connects one input to the output. It has **passive components** forming a low pass filter connected to a transmitter input of the switch. The **passive components** are constituents of a multilayer ceramic passive module with a base body of stacked dielectric and electrically conducting layers. The switch is on the upper or lower side of the body.
DETAILED DESCRIPTION - The module has a voltage-controlled switch (1) with transmitter and receiver inputs (2,3) and an output (4) and selectively connects one of the inputs to the output. It has **passive components** forming a low pass filter (5,6) **electrically connected** to a transmitter input of the switch. The **passive components** are constituents of a multilayer ceramic passive module with a base body of stacked dielectric and electrically conducting layers. The switch is mounted on the upper or lower side of the base body. INDEPENDENT CLAIMS are also included for the following: the use of an inventive circuit module as the front-end module in a mobile radio device.
USE - For use as the front-end module in a mobile radio device.
ADVANTAGE - The circuit consumes very low current and occupies little space.
DESCRIPTION OF DRAWING(S) - The drawing shows a schematic block diagram representation of an inventive switch module
bandpass filter 10-12
voltage-controlled switch 1
transmitter and receiver inputs 2,3
output 4
low pass filters 5,6
Dwg.1/3

L38 ANSWER 2 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 2002-465636 [50] WPIX
DNN N2002-367047 DNC C2002-132663
TI Microparticle coating method for anisotropic electroconductive adhesive, involves coating microparticle having preset particle diameter, aspect ratio, coefficient of variation with resin coating substance.
DC A85 G03 L03 P53 U11 X12
PA (SEKI) SEKISUI CHEM IND CO LTD
CYC 1
PI JP 2002052333 A 20020219 (200250)* 9p

ADT JP 2002052333 A JP 2000-241316 20000809
PRAI JP 2000-241316 20000809
AB JP2002052333 A UPAB: 20020807
NOVELTY - The microparticle coating method involves preparing mixture containing microparticle, coating substance comprising resin soluble in water and dispersion medium, and removing dispersion medium by volatilization. The microparticle has an average particle diameter (APD) of 0.2-3000 mu m, aspect ratio less than 5 and coefficient of variation of 40% or less. The thickness of coating layer is less than 1/4 of APD.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: (i) Coating microparticle coated using coating method; (ii) Anisotropic electroconductive adhesive having coating microparticle dispersed in resin binder; (iii) Anisotropic electroconductive joining film having coating microparticle dispersed in resin binder; (iv) Electroconductive connection structure object, which has electrode portion or **electric device** component, **bonded** on the substrate through coating microparticle. The conduction of electrode portions is achieved by destroying the microparticle coating layer by heating and/or pressurization and contacting electrical conducting material of coating microparticle with electrode portions.

USE - For coating the microparticle for anisotropic electroconductive adhesive, anisotropic electroconductive joining film, electroconductive connection structure object (all claimed), and for connecting fine electrodes, active components such as transistor and diode, and **passive components** such as capacitor and crystal resonator on the substrate.

ADVANTAGE - Efficiency of coating method is high, as it does not generate a microparticle without coat. The microparticle having high specific gravity and wettability is also coated. The coating layer has uniform thickness as thickness of coating layer is controlled easily. Generation of multiple particles is reduced. The coating microparticle has low connection resistance and high **electrical** capacitance during **connection**. The leak phenomenon does not occur between adjacent electrodes.

Dwg.0/0

L38 ANSWER 3 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 2001-417508 [44] WPIX
CR 2000-364743 [27]; 2001-031644 [65]; 2001-112070 [03]; 2001-299518 [65]
DNN N2001-309371 DNC C2001-126084
TI Tamper-resistant wireless article, e.g. tag, includes **electronic device** attached to substrate by strong adhesive, and pattern of electrically conductive material having elongated electrical conductor and electrical contact.
DC A85 L03 W02
IN CHUNG, K K
PA (AMER-N) AMERASIA INT TECHNOLOGY INC
CYC 23
PI WO 2001026180 A1 20010412 (200144)* EN 59p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CN JP KR SG US
CN 1323505 A 20011121 (200218)
ADT WO 2001026180 A1 WO 2000-US27227 20001003; CN 1323505 A CN 1999-812227 19991014
PRAI US 2000-212401P 20000619; US 1999-411849 19991004; US 1999-412058 19991004; US 1999-169790P 19991209; US 1998-104337P 19981015; US 1999-129497P 19990415; US 1999-131377P 19990428; US 1999-134656P 19990518
AB WO 200126180 A UPAB: 20020221
NOVELTY - A tamper-resistant wireless article, comprises a substrate having layer(s) of dielectric adhesive for attaching to object; a pattern

of electrically conductive material comprising elongated electrical conductor on one surface of the substrate and electrical contact(s); and an **electronic device**(s) attached to the substrate by strong adhesive and comprising electrical contact(s).

DETAILED DESCRIPTION - A tamper-resistant wireless article consists of substrate (20), pattern of electrically conductive material, and at least one **electronic device** (40). The substrate includes layer(s) of dielectric adhesive having an exposed surface for attaching the substrate to an object. The pattern of the electrically conductive material comprises an elongated electrical conductor (30) on one surface of the substrate and electrical contact(s). The **electronic device** is attached to the substrate by a strong adhesive and comprises contact(s) (42, 44) electrically connected to the contact of electrically conductive material pattern. The strong dielectric adhesive of substrate or the strong adhesive attaching the **electronic device** renders the article resistant to tampering.

USE - As electronic article, e.g. tag, identification badges, and smart cards.

ADVANTAGE - The article shows evidence of and/or resists tampering, and is simple and inexpensive to make.

DESCRIPTION OF DRAWING(S) - The figures are plan views of the electronic article.

Substrate 20

Elongated electrical conductor 30

Electronic device 40

Electronic device contacts 42, 44

Dwg.1, 2/17

L38 ANSWER 4 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 2000-627845 [60] WPIX
DNN N2000-465173 DNC C2000-188037
TI Isolation of **electrical devices** useful in metal-oxide semiconductor field effect transistor structures, involves incorporating an element into a conductive layer formed over an insulating layer.
DC L03 U11 U12 U13
IN KRISHNAN, S
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 6117745 A 20000912 (200060)* 8p
ADT US 6117745 A Provisional US 1997-57964P 19970905, US 1998-148260 19980904
PRAI US 1997-57964P 19970905; US 1998-148260 19980904
AB US 6117745 A UPAB: 20001123

NOVELTY - An **electrical device** on a semiconductor substrate is isolated from a structure that collects charges by incorporating an element into a conductive layer which is formed over an insulating layer. The element is incorporated to render the conductive layer more resistive.

DETAILED DESCRIPTION - Isolation of an **electrical device** over a semiconductor substrate from a structure which collects charges involves:

(a) forming an insulating layer on the substrate;

(b) forming a conductive layer on the insulating layer;

(c) incorporating at least one element into a portion of the conductive layer so as to render that portion more resistive; and

(d) rendering conductive the rendered more **resistive conductive** layer after one or more charging events by subjecting the portion of the conductive layer to an elevated temperature.

USE - The method is used for isolating an **electrical device** useful in a metal oxide semiconductor field effect transistor (MOSFET) structure.

ADVANTAGE - The **electrical device** is protected from charge-induced damage. The process steps which cause the most charging damage can be determined.
Dwg.0/6

L38 ANSWER 5 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 2000-086827 [07] WPIX
DNN N2000-068143 DNC C2000-024187
TI Electrosurgical instrument, for e.g. cutting and cauterizing tissue.
DC A96 P31 S05
IN BACICH, S; NARDELLA, P C; NGUYEN, T N; TON, D T; VIDYARTHI, P; WRUBLEWSKI, T A
PA (CONC-N) CONCEPTUS INC; (MEDI-N) MEDICAL SCI INC
CYC 22
PI WO 9962414 A1 19991209 (200007)* EN 33p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: AU CA JP
AU 9945455 A 19991220 (200021)
US 6080152 A 20000627 (200036)
ADT WO 9962414 A1 WO 1999-US12305 19990603; AU 9945455 A AU 1999-45455 19990603; US 6080152 A US 1998-92694 19980605
FDT AU 9945455 A Based on WO 9962414
PRAI US 1998-92694 19980605
AB WO 9962414 A UPAB: 20000209
NOVELTY - **Electrosurgical device** (10) comprises:
(A) a frame having a proximal end (22) and a distal end (24);
(B) an electrode assembly coupled to the distal end of the frame; and
(C) a nonconductive body mechanically interlocked with the electrode (12) so that the gap is formed between the electrode and the nonconductive body.
USE - Used for cutting and cauterizing tissue. It is suitable for insertion into the patient with close surgery such as arthroscopic, endoscopic, hysteroscopic, urologic, resectoscopic and laproscopic procedures. It is also used in open surgery. It is to be used in an environment that includes and isotonic fluid. The invention can be used with a delivery instrument other than the hysteroscope.
ADVANTAGE - The conductive surface of the active electrode in contact with surrounding fluid is reduced and minimized the current dissipation into the surrounding fluid. Thus, the electrosurgical instrument enables the effective use of monopolar electrosurgical tools in an isotonic fluid medium. The invention maximizes the coated area of the electrode while minimizes the non-coated, tissue affecting portion.
DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a monopolar instrument having a selectively coated electrode.
Electrosurgical instrument 10
Active electrode 12
Probe 20
Proximal end 22
Distal end 24
Energy source 50
Conductors 54, 56
Dwg.1/12

L38 ANSWER 6 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1999-600419 [51] WPIX
DNN N1999-442554 DNC C1999-174748
TI Resettable fuse composition for **electronic circuit** protection.
DC A28 A35 A60 A85 L03 U24 X12 X13
IN EKIS, J J; OSUNA, J E; POINTER, B T; STYGAR, V E
PA (FECO) FERRO CORP

CYC 1
PI US 5963121 A 19991005 (199951)* 6p
ADT US 5963121 A US 1998-190032 19981111
PRAI US 1998-190032 19981111
AB US 5963121 A UPAB: 19991207
NOVELTY - A resettable fuse (15) comprises the reaction product of a polyethylene glycol and a diepoxide plus conductive particles applied as a solution between terminals (20) onto a substrate (12) and cured by heating.

DETAILED DESCRIPTION - A resettable fuse comprises a fuse section (15) between two silver-filled epoxy resin terminals (20) on a substrate (12) comprising a mixture of the reaction product of polyethylene glycol and a diexpoxide having a molecular weight of at least 18,000, conductive particles, solvent and volatility adjusters. The mixture is applied to the substrate between the terminals and heated to flash off solvent and cure the reaction product.

USE - As a resettable fuse (claimed) for **electronic circuit** protection devices

ADVANTAGE - The fuse resets itself and does not need replacement, the problems of PTC devices are avoided and fuses can be screen printed onto printed circuits; the switching temperature is stable over time and use.

DESCRIPTION OF DRAWING(S) - A cross-section of the fuse is shown.
Substrate 12
Fuse 15
Dwg.1/1

L38 ANSWER 7 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1999-589773 [50] WPIX
DNN N1999-434865
TI Packaging structure for multilayered microelectronic device in desk top computer.
DC T01 V04
IN HAYDEN, W W; WILLIAMS, R L
PA (RAYT) RAYTHEON CO
CYC 1
PI US 5963426 A 19991005 (199950)* 11p
ADT US 5963426 A US 1997-858640 19970519
PRAI US 1997-858640 19970519
AB US 5963426 A UPAB: 19991201
NOVELTY - Each module assembly (22a-22d) has an **electronic circuit** (24) formed on the electrical interconnect locations (26). The circuit elements (60) in each module are positioned in registry. A direct straight line connection is provided between facing circuit element with direct electrical interconnector (66).

DETAILED DESCRIPTION - Several parallelly arranged module assemblies (22a-22d) are affixed to a support (28), which inturn is affixed to a thermally conductive heat sink (30). Chips (60) and **passive components** are provided in each module. The circuit elements are spaced apart by a distance of 0.050 inches. The circuit elements are disposed in a housing (64) which is in direct thermal contact with the heat sink.

USE - For multi-layered microelectronic devices in desk top computer and controllers.

ADVANTAGE - Reduces electrical path lengths between modules by providing straight line **connection** with direct **electrical** interconnectors. Heat sink is in close proximity to circuit elements and in direct thermal contact with housing of module assemblies, thus cooling efficiency is improved. Separation of various subsystems into modules, minimizes possible interference due to electrical signals and heat production.

DESCRIPTION OF DRAWING(S) - The figure shows schematic sectional

view of packaging structure.
Module assemblies 22a-22d
Electronic circuit 24
Electrical interconnect locations 26
Support 28
Heat sink 30
Chip 60
Housing 64
Interconnector 66
Dwg.4/8

L38 ANSWER 8 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1999-492833 [41] WPIX
DNN N1999-367010
TI Component module for use with printed wiring board.
DC V04
IN SATWINDER, M
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 5936840 A 19990810 (199941)* 8p
ADT US 5936840 A US 1997-963142 19971103
PRAI US 1997-963142 19971103
AB US 5936840 A UPAB: 19991011
NOVELTY - Several components (21,23,25,27,29), each with a pair of contacts (21a,21b) are formed into a single module (20) with several insulating spacers (22,24,26,28) between components. The contacts (21a,21b) are **electrically connected** to the respective printed wiring board conductors.
DETAILED DESCRIPTION - The insulating spacers (22,24,26,28) are provided between the adjacent components (21,23,25,27,29) and the spacer serves to insulate adjacent components from each other and secures the component together to form the module (20).
USE - For combining several components for use with printed wiring board used in hand-held **electronic devices** and portable computers.
ADVANTAGE - As the components are interconnected with each other, only less mounting area is required on the printed wiring board, therefore more modules and devices are mounted on the printed wiring board. With the components in module form, less space is required for all the components and the conductors interconnecting the components are shorter and require less space allowing for higher component density for the printed wiring board.
DESCRIPTION OF DRAWING(S) - The figure shows stacked array of **passive components**.
Single module 20
Components 21,23,25,27,29
Contacts 21a,21b
Insulating spacers 22,24,26,28
Dwg.3/8

L38 ANSWER 9 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1999-240748 [20] WPIX
DNN N1999-180014
TI Surge absorption element for protecting **electronic circuit** - has mold layer whose relative density is larger than that of **non-conductive ceramic** sintered compact formed on it.
DC U24 V01
PA (TOHM) TOKIN CORP
CYC 1
PI JP 11069613 A 19990309 (199920)* 6p

ADT JP 11069613 A JP 1997-241918 19970822
PRAI JP 1997-241918 19970822
AB JP 11069613 A UPAB: 19990603
NOVELTY - A mold of surge absorption layer, between which a **non-conductive ceramic** sintered compact is formed whose relative density is lower than that of mold layer. The mold layer is interposed between the mutually opposing internal electrodes (3). DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of surge absorption element.
USE - For protecting **electronic circuit** of electronic machine from overvoltage, etc.
ADVANTAGE - By eliminating need for complicated structure, size is reduced. DESCRIPTION OF DRAWING(S) - The figure shows sectional view of production procedure of surge absorption element. (3) Internal electrodes.
Dwg.1/2

L38 ANSWER 10 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1999-045447 [04] WPIX
DNN N1999-033119 DNC C1999-014311
TI Electrosurgical instruments for cutting and cauterising tissue in isotonic solutions - has frame coupled to either electrode partly covered with insulating coating or coupled to insulating body with conductive coating forming electrode.
DC A96 P31
IN BACICH, S R; NARDELLA, P C; NGUYEN, T N; TON, D T; VIDYARTHI, P; WRUBLEWSKI, T A; N'GUYEN, T N
PA (MEDI-N) MEDICAL SCI INC; (CONC-N) CONCEPTUS INC
CYC 22
PI WO 9855037 A1 19981210 (199904)* EN 37p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: AU CA JP
AU 9877277 A 19981221 (199919)
US 6071283 A 20000606 (200033)
ADT WO 9855037 A1 WO 1998-US11720 19980605; AU 9877277 A AU 1998-77277 19980605; US 6071283 A Provisional US 1997-49363P 19970606, US 1998-92609 19980605
FDT AU 9877277 A Based on WO 9855037
PRAI US 1997-49363P 19970606; US 1998-92609 19980605
AB WO 9855037 A UPAB: 19990127
An **electrosurgical device** has an electrode (12) coupled to a frame. Part of the electrode has an insulating coating. 1) In use the uncoated part of the electrode applies electrosurgical energy to body tissue. 2) The electrode is coupled to the distal end of the frame. 3) In a modification of 2 the electrode is a conductive coating on a non-conductive body coupled to the frame.
The insulating coating may be ceramic, glass, aluminum silicate, alumina, boron, **non-conductive** epoxy, **ceramic** adhesive, glass enamel, glass filled polymer, polysulfone, polytetrafluoroethylene, polysiloxane, silicone, polyetheretherketone, 'Parylene' (RTM) or 'Kevlar' (RTM).
USE - Electrosurgical instruments for cutting and cauterising tissue in arthroscopy, endoscopy, hysteroscopy, laparoscopy, resectoscopy, etc.
ADVANTAGE - The instrument can be used in isotonic solutions.
Dwg.1/8

L38 ANSWER 11 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1998-107472 [10] WPIX
DNN N1998-086453
TI Compound circuit substrate for mounting active and **passive components** of **electronic circuit** of portable telephone, PHS, computer, electronic notebooks - includes first and second

resin made substrates, ceramic substrate and metallic substrate on whose either surfaces, passive and active circuit components are mounted.

DC V04
PA (MATU) MATSUSHITA DENKI SANGYO KK
CYC 1
PI JP 09331132 A 19971222 (199810)* 6p
ADT JP 09331132 A JP 1996-150621 19960612
PRAI JP 1996-150621 19960612
AB JP 09331132 A UPAB: 19980309
The circuit substrate includes a first resin made substrate onto which a second resin made substrate, a ceramic substrate and a metallic substrate are mounted and are **electrically connected**.

The **passive components** such as resistor, capacitor, inductor and active components such as transistor, IC are mounted on either of the above substrates.

ADVANTAGE - Performs high density mounting at low cost. Simplifies structure. Attains desired characteristics.
Dwg.1/5

L38 ANSWER 12 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1998-093454 [09] WPIX
DNN N1998-074686
TI Double sided multilayered printed circuit for mounting electronic component e.g. LSI, **passive component** used in **electronic device** - includes wiring pattern formed on both sides of substrate and predetermined parts of wiring pattern are electrically contacted to conductive resin composition.
DC V04
IN NAKATANI, S
PA (MATU) MATSUSHITA DENKI SANGYO KK; (MATU) MATSUSHITA ELECTRIC IND CO LTD
CYC 2
PI JP 09321399 A 19971212 (199809)* 11p
US 5888627 A 19990330 (199920)
JP 3197213 B2 20010813 (200148) 10p
ADT JP 09321399 A JP 1996-134023 19960529; US 5888627 A US 1997-865055 19970529; JP 3197213 B2 JP 1996-134023 19960529
FDT JP 3197213 B2 Previous Publ. JP 09321399
PRAI JP 1996-134023 19960529
AB JP 09321399 A UPAB: 19980302
The printed circuit includes a sheet substrate (100) which is made of an organic non-woven fabrics material with density more than 0.8g/cm3. An insulating resin composition layer (101) is provided on both sides of the substrate respectively. A cover film (102) covers the insulating resin composition layers respectively. A through hole (103) is formed at predetermined positions of the substrate. A conductive resin composition (104) is filled up into the through holes.

Wiring patterns (106) formed on both sides of the substrate at predetermined positions and predetermined parts of the wiring pattern are **electrically connected** to the conductive resin composition.

ADVANTAGE - Improves reliability. Offers reliable printed circuit. Avoids influence on wiring pattern due to organic non- woven fabric material thereby enables to contact insulating resin layer firmly. Reduces twisting of substrate. Provides stable connection between wiring pattern and conductive resin composition. Improves electric insulating withstand breakdown voltage, greatly. Simplifies manufacturing process.
Dwg.1/4

L38 ANSWER 13 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1997-138381 [13] WPIX
DNN N1997-114377

TI **Electronic device** equipped with IC, LSI, component mounted onto circuit substrate - in which resin is applied along circumference of semiconductor element, and between substrate and semiconductor element.
DC U11 U14
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 09017913 A 19970117 (199713)* 8p
ADT JP 09017913 A JP 1995-163389 19950629
PRAI JP 1995-163389 19950629
AB JP 09017913 A UPAB: 19970326
The device (10) consists of a semiconductor element that is installed on a wiring board (1) using a solder (5). A component space of 5mm or less is formed between the adjoining semiconductor elements. A **passive component** (7) is installed on a substrate by an **electrically** conductive **connection** member.
Resin (6) is arranged along circumference semiconductor element and between the substrate and semiconductor element.
ADVANTAGE - Prevents generation of poor connection of passive chip component at time of re-heat. Improves reliability of device, remarkably. Increases industrial value.
Dwg.1/8

L38 ANSWER 14 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1997-042232 [04] WPIX
DNN N1997-035173 DNC C1997-013295
TI Electrically heated ice cube tray to provide release of ice cubes - in which tray is heated by current through a conductive polymer, such as high density polyethylene contg. carbon black..
DC A23 A26 A85 L03 Q75 X25 X27
IN HYGEMA, T L; SMITH, K W
PA (HEAT-N) HEATERS ENG INC
CYC 1
PI US 5582754 A 19961210 (199704)* 12p
ADT US 5582754 A CIP of US 1993-163928 19931208, US 1995-374895 19950119
PRAI US 1995-374895 19950119; US 1993-163928 19931208
AB US 5582754 A UPAB: 19970122
Tray (10) has an electrically insulating body portion (34) with compartments (12) to receive liquid to be frozen, and an electrically **resistive conductive** polymer member (36), shaped to conform to the compartments and arranged between a first (28) and a second (30) electrode grids arranged so that, when connected in an **electrical circuit**, a substantially uniform current density flows through the conductive polymer (36) to provide uniform heating thereof. The resistance of the conductive polymer changes as a function of its temperature.
USE - Used esp. as an ice tray in an automatic ice making machine.
ADVANTAGE - Construction provides uniform heating of the tray surfaces ensuring rapid release of the ice at minimum power.
Dwg.1/4

L38 ANSWER 15 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1996-370698 [37] WPIX
CR 1996-476283 [47]
DNN N1996-311873 DNC C1996-117587
TI Solder pad for bonding **electronic device** to ceramic substrate - comprising solder pad portion of conductive **ceramic** runner on **non-conductive ceramic** substrate with solder wettable layer attached to pad portion.
DC L03 M23 U11 U14 V04
IN CARSON, R T; HOGREFE, A W; RECKLEBEN, L

PA (MOTI) MOTOROLA INC
CYC 1
PI US 5543583 A 19960806 (199637)* 9p
ADT US 5543583 A Div ex US 1994-331465 19941031, US 1995-542122 19951012
PRAI US 1994-331465 19941031; US 1995-542122 19951012
AB US 5543583 A UPAB: 19961202
Electronic device is bonded to a ceramic substrate (130) using a conductive solder pad (110) portion of a conductive runner (120) on the non-conductive substrate. The conductive runner consists of a conductive ceramic material, pref. a layer of InSn oxide. A solder wettable layer is attached to the solder pad portion and consists of at least 50 wt .% In.
ADVANTAGE - Provides reliable low cost bond between metallic and ceramic conductors.
Dwg.1/10

L38 ANSWER 16 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1996-009576 [01] WPIX
DNN N1996-008357
TI Windscreen wiper de-icing windscreen construction method - forming **resistive conductive** coatings heat generating circuit along glass panel bottom edges to deice wiper in at-rest position.
DC X22 X25
IN GOLD, P
PA (GOLD-I) GOLD P
CYC 2
PI US 5467522 A 19951121 (199601)* 5p
CA 2152098 A 19960226 (199624)
ADT US 5467522 A US 1994-295410 19940825; CA 2152098 A CA 1995-2152098 19950619
PRAI US 1994-295410 19940825
AB US 5467522 A UPAB: 19960108
The method involves stacking a number of windscreens each consisting of glass laminates with an inbetween plastic ply in superposed relation and simultaneously applying to the stacked windscreens an electrically conductive coating along bottom edges of the glass laminates.
The coated edges are integrated into an **electrical circuit** to be electrically connected to a battery of the auto. A windscreen wiper is installed on each removed windscreen. At the starting position of transversing movement the windscreen wiper is at rest above a marginal edge of the windscreen heated by the battery-operated **electric circuit** so as to cause a deicing of the windscreen wiper.
ADVANTAGE - Has deicing function and minimises shattering.
Dwg.1,4/4

L38 ANSWER 17 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1995-392673 [50] WPIX
CR 1995-327310 [42]; 1998-009167 [01]; 1998-009168 [01]; 1998-031234 [03]; 2002-235045 [54]
DNN N1995-286301
TI Ceramic microelectronic package for high frequency **electronic devices** - has ceramic circuit substrate with cavity and several conductive patterns, ceramic seal ring substrate with larger cavity and ceramic lid that is electrically isolated from base which acts as single ground plane.
DC U11
IN ANDERSON, P M; BABIARZ, J; GOETZ, M; LINDNER, A W; WEIN, D S
PA (STRA-N) STRATEDGE CORP
CYC 1
PI US 5465008 A 19951107 (199550)* 9p

ADT US 5465008 A US 1993-134269 19931008
PRAI US 1993-134269 19931008
AB US 5465008 A UPAB: 20020508
The ceramic microelectronic package comprises a base (102) with a conductive top and bottom surface. A ceramic circuit substrate (106) has a first cavity with several conductive patterns deposited on the surface. The ceramic circuit substrate is attached to the top of the base.

A ceramic seal ring substrate (110) with a second cavity which is larger than the first cavity is attached to the ceramic circuit substrate by a **non-conductive** element. A **ceramic** lid (114) is attached to the ceramic seal ring substrate and the base acts as a single ground plane which is electrically isolated from the ceramic lid.

USE/ADVANTAGE - For electronic interconnection housing for high frequency **electronics devices** and components. Uses minimum of conductive materials. Eliminates superfluous electrical conductors. Has relatively uniform dielectric constant.
Dwg.1/6

L38 ANSWER 18 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1995-081627 [11] WPIX
CR 1993-327520 [41]
DNN N1995-064638
TI Multilayer **electric circuit** having partially embedded external connection pins - has electrical stripline formed on thermally fusible sheet (10), and partly extending adjacent to sheet edge, with sheet being fused to another contg. cavity for retaining pin.
DC U14 V04
IN MARTIN, F J; MIEHLS, D J; POND, R G
PA (HUGA) HUGHES AIRCRAFT CO
CYC 1
PI US 5386085 A 19950131 (199511)* 9p
ADT US 5386085 A Div ex US 1991-785859 19911031, US 1993-88964 19930702
FDT US 5386085 A Div ex US 5249355
PRAI US 1991-785859 19911031; US 1993-88964 19930702
AB US 5386085 A UPAB: 19950322
The multilayer **electrical circuit** structure, has a first sheet of electrically **nonconductive ceramic** tape having a stripline formed on it, and partly extending adjacent to one edge. A second sheet of similar material has a cavity formed through it, which opens at one edge of the second sheet. A third sheet has an edge aligned with the those the first and second sheets, and all three are adhered together with their edges aligned. The cavity is aligned with, and exposes the portion of the stripline and the cavity is enclosed by the first sheet and the third sheet except at the edge where the cavity is open, which provides an opening in the structure.

An electrically conductive pin having a first portion extending through the opening and into the cavity, and is ohmically adhered to the portion of the stripline, and a second portion remains external of the structure for external electrical connection with other elements. The three sheets are thermally fused together.

ADVANTAGE - Enables fabrication of self contained interconnectable hermetic high frequency LTCC modules. Increases feasibility of module-to-module interconnections which occupy less area.
Dwg.2/12

L38 ANSWER 19 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1993-134211 [16] WPIX
CR 1995-184450 [24]; 1998-144763 [13]; 1998-506382 [43]; 1999-094783 [08]
DNN N1993-102330 DNC C1993-059889
TI Electroconductive adhesive compsns. - comprise solder powder, protected crosslinking agent and reactive monomer or polymer, used for attaching

electrical components to **electrical circuits**.
DC A85 L03 M23 P42 P55 U11 V04 X12
IN CAPOTE, M A; CRAIG, H P; MANESIS, N J; TODD, M G
PA (TORA-N) TORANAGA TECHNOLOGIES INC; (CAPO-I) CAPOTE M A; (CRAI-I) CRAIG H P; (MANE-I) MANESIS N J; (TODD-I) TODD M G
CYC 30
PI WO 9306943 A1 19930415 (199316)* EN 42p
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE
W: AU BG BR CA CS FI HU JP KR NO PL RO RU
AU 9227678 A 19930503 (199334)
US 5376403 A 19941227 (199506) 18p
EP 646048 A1 19950405 (199518) EN
R: AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL SE
JP 07502369 W 19950309 (199518) 14p
AU 663342 B 19951005 (199547)
US 5830389 A 19981103 (199851)
KR 9710170 B1 19970621 (199945)
JP 2972338 B2 19991108 (199952) 25p
ADT WO 9306943 A1 WO 1992-US8333 19921001; AU 9227678 A AU 1992-27678 19921001; US 5376403 A CIP of US 1990-477678 19900209, US 1991-769892 19911001; EP 646048 A1 EP 1992-921540 19921001, WO 1992-US8333 19921001; JP 07502369 W WO 1992-US8333 19921001, JP 1993-507034 19921001; AU 663342 B AU 1992-27678 19921001; US 5830389 A CIP of US 1990-477678 19900209, Div ex US 1991-769892 19911001, US 1994-324060 19941017; KR 9710170 B1 WO 1992-US8333 19921001, KR 1994-701007 19940329; JP 2972338 B2 WO 1992-US8333 19921001, JP 1993-507034 19921001
FDT AU 9227678 A Based on WO 9306943; EP 646048 A1 Based on WO 9306943; JP 07502369 W Based on WO 9306943; AU 663342 B Previous Publ. AU 9227678, Based on WO 9306943; US 5830389 A Div ex US 5376403; JP 2972338 B2 Previous Publ. JP 07502369, Based on WO 9306943
PRAI US 1991-769892 19911001; US 1990-477678 19900209; US 1994-324060 19941017
AB WO 9306943 A UPAB: 19991210
Compsn. comprises solder powder; chemically protected cross-linking agent (I) with fluxing properties; and a reactive monomer or polymer. The solder is pref. Sn, Bi, Pb, Cd, Zn, Ga, In, Te, Hg, Tl, Se, Sb or Po or alloys of these, esp. Sn63Pb37.

(I) is pref. an acid or strong base protected to become reactive at or near the time the solder powder is melted.

USE/ADVANTAGE - As a conductive adhesive for attaching components and for forming conductive paths on printed circuits, etc. Compsn. has a conductivity approaching that of Cu metal, good solderability, high adhesive strength to Cu clad **FR4** epoxy PCB laminates and high corrosion resistance.
Dwg.1/4

L38 ANSWER 20 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1993-126287 [15] WPIX
DNN N1993-096404
TI High power hermetic package for **electrical device** - includes aluminium nitride substrate with copper thick film ink screen printed on it and kovar ring brazed to copper thick film ink and cover bonded to ring.
DC U11
IN IBRAHIM, S S
PA (CTSC) CTS CORP
CYC 1
PI US 5198885 A 19930330 (199315)* 4p
ADT US 5198885 A US 1991-701492 19910516
PRAI US 1991-701492 19910516
AB US 5198885 A UPAB: 19930924

The base planar electrically **non-conductive ceramic** substrate having a first electrical conductor patterned on it. A covering device is adhered to the substrate. The covering device and the substrate forms an hermetic enclosure. A first electrical component, relatively more thermally dissipating than said first electrical conductor is electrically connected to the first electrical conductor and hermetically contained within the covering device and the substrate. The covering device has a flange extending in a direction parallel to the planar substrate beyond the planar substrate. The flange is configured for securement to the supporting structure. The flange has a resilient member to deform preferentially to a remainder of the flange when the package is secured to the supporting structure. ADVANTAGE - Uses minimum number of interfaces between semiconductor device and heat sink.
2/3

L38 ANSWER 21 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1992-134112 [17] WPIX
DNN N1992-100081 DNC C1992-062709
TI Self-heating filter element for aerosol analysis - has star-shaped, cross-sectional stainless steel plates which are heated by direct passage of electricity.
DC J01 X25
IN AUFFRET, J C; CLARAMONTE, M; AUFFRET, J
PA (NRDA) SOC NAT IND AEROSPATIALE; (NRDA) AEROSPATIALE
CYC 5
PI EP 481858 A 19920422 (199217)* FR 10p
R: DE ES GB IT
FR 2667798 A1 19920417 (199223) 17p
EP 481858 B1 19950719 (199533) FR 11p
R: DE ES GB IT
DE 69111365 E 19950824 (199539)
ES 2076491 T3 19951101 (199550)
ADT EP 481858 A EP 1991-402724 19911011; FR 2667798 A1 FR 1990-12678 19901015; EP 481858 B1 EP 1991-402724 19911011; DE 69111365 E DE 1991-611365 19911011, EP 1991-402724 19911011; ES 2076491 T3 EP 1991-402724 19911011
FDT DE 69111365 E Based on EP 481858; ES 2076491 T3 Based on EP 481858
PRAI FR 1990-12678 19901015
AB EP 481858 A UPAB: 19931006
Filter element, is of annular, star-shaped cross-section, comprising generally radial, flat plates (6) of porous stainless steel which are heated by direct passage of electricity. Plates (6) are connected alternately at radially inner and outer edges, by **non-conducting ceramic** sealing strips (12,14), and alternately at the axial ends of the element by further porous stainless steel sections (16,32), except for one non-conducting section (34) between electric terminals (28,30). This provides an **electric circuit** between the terminals, running axially up and down alternate plates (6)..

USE/ADVANTAGE - In analysis of planetary atmospheres in exploration of the solar system. Compared with filter elements with separate heaters, the element saves weight, space and power.
(1/6)
1/6

L38 ANSWER 22 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1990-148778 [20] WPIX
DNN N1990-115324
TI Hybrid integrated electronic control unit with heat sink - has control, power and timing components integrated in hybrid circuit and bonded to single ceramic carrier.
DC Q54 U14 V04 X22

IN KILIAN, H; LEICHT, G; NIEMETZ, L
PA (TELE) TELEFUNKEN ELECTRONIC GMBH; (TELE) TEMIC TELEFUNKEN MICROELECTRONIC GMBH
CYC 5
PI DE 3837975 A 19900510 (199020)*
EP 368143 A 19900516 (199020)
R: DE FR GB IT
US 5159532 A 19921027 (199246) 4p
ADT DE 3837975 A DE 1988-3837975 19881109; EP 368143 A EP 1989-120280 19891102; US 5159532 A Cont of US 1989-433986 19891109, US 1991-707198 19910528
PRAI DE 1988-3837975 19881109
AB DE 3837975 A UPAB: 19940407
The **electronic circuit** (1) is mounted on a ceramic carrier (5), pref. of Al203 for electrical insulation from its heat sink (15). Its components comprise a control section (2), a power section (3) and a resistance-capacitance combination (4). Plug connections (12, 13) are wire-bonded (14) to the circuit from a metallic plate (11) integrated into the plastic housing (6) to afford circuit contacts with the possibility of external connection via a socket (8).

Conductive tracks and resistances are printed by thick-film technology on the carrier to which surface mount components and chips are bonded with solder paste. The circuit can undergo functional tests before being bonded to its heat sink.

USE/ADVANTAGE - Transistorised automotive ignition systems. Assembly is simplified, cost of mfr. is reduced and vol. of structure is made smaller. @(4pp Dwg.No.1/2)@

USE/ADVANTAGE - Transistorised automotive ignition systems. Assembly is simplified, cost of mfr. is reduced and vol. of structure is made smaller.
1/2

L38 ANSWER 23 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1987-266144 [38] WPIX
DNN N1987-199457
TI Nonlinear position transducer e.g. for electronic injection system - uses A to D converter to detect position of valve controlling rate of flow of air inducted to cylinder.
DC Q52 S02 X22
IN DECONCINI, R
PA (WEBE) WEBER SRL
CYC 5
PI GB 2188160 A 19870923 (198738)* 4p
DE 3709028 A 19870924 (198739)
FR 2596147 A 19870925 (198743)
US 4762108 A 19880809 (198834) 4p
GB 2188160 B 19891115 (198946)
IT 1187977 B 19871223 (199044)
ADT GB 2188160 A GB 1987-706396 19870318; DE 3709028 A DE 1987-3709028 19870319; US 4762108 A US 1987-28315 19870320
PRAI IT 1986-67226 19860321
AB GB 2188160 A UPAB: 19930922
The transducer (1) comprises a means (5) for detecting the position ( ) of valve (7), and second means (3,4) coupled to the first and operable to provide an electrical output signal (V2) in non-linear relationship with the position (Alpha) of the valve and in which these second means comprise an **electrical circuit** having only **passive components**.

The first means comprises a potentiometer having a linear characteristic the cursor (6) of which is coupled to the valve and **electrically connected** to an intermediate node of series

connected resistors (3,4) connected in parallel with the potentiometer and constituting the second means. The electrical output signal from the second means is supplied to an A to D converter.
ADVANTAGE - Accurate.
1/2

L38 ANSWER 24 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1987-222531 [32] WPIX
DNN N1987-166382 DNC C1987-093571
TI Multilayer **electric circuit** prodn. - on base board, using platable copper paste as base for producing second copper layer by plating.
DC A85 L03 V04
IN IWASA, Y
PA (ASAH-N) ASAHI CHEM RES LAB
CYC 7
PI DE 3700912 A 19870806 (198732)* 12p
GB 2186433 A 19870812 (198732)
GB 2186435 A 19870812 (198732)
JP 62163302 A 19870720 (198734)
JP 62163387 A 19870720 (198734)
FR 2593015 A 19870717 (198735)
NL 8700053 A 19870803 (198735)
US 4724040 A 19880209 (198809) 13p
DE 3700912 C 19890706 (198927)
GB 2186433 B 19900214 (199007)
GB 2186435 B 19900214 (199007)
KR 9003158 B 19900509 (199120)
JP 03050405 B 19910801 (199135)
ADT DE 3700912 A DE 1987-3700912 19870114; GB 2186433 A GB 1987-716 19870113; GB 2186435 A GB 1987-718 19870113; JP 62163302 A JP 1986-5643 19860114; JP 62163387 A JP 1986-5644 19860114; FR 2593015 A FR 1987-273 19870113; NL 8700053 A NL 1987-53 19870112; US 4724040 A US 1986-940733 19861211; JP 03050405 B JP 1986-5643 19860114
PRAI JP 1986-5643 19860114; JP 1986-5644 19860114
AB DE 3700912 A UPAB: 19930922
In prodn. of **electric circuits** on a base board, a Cu layer is fixed to one side of the base board; the Cu layer is etched to form a no. of first **electric circuits**; this side of the base board is covered with plating resist apart from the areas which are to be **connected electrically** to other circuits, which are to be formed on the first layer; an electroconductive Cu paste, suitable for metal plating, is applied to this side of the base board so that the first circuits of the first layer can be sub-divided into at least two zones, which can be electrically insulated from one another; hardening is carried out by heating the base boards.
The base board is cleaned; the base board is dipped in a metal plating soln. to form a metal plating film on the Cu paste, to give at least two circuits of a second layer of plating film and Cu paste; pt. of each of the insulated areas of the circuits of the second layer is coated with electroconductive paste; the base board is heated to cure this paste to provide a pair of terminals; an electrical resistor paste with predetermd. resistance is applied to a section between the 2 terminals; and the base board is heated to cure the resistor paste.
USE/ADVANTAGE - The process utilises newly developed Cu pastes with esp. good metal plating property.
1/6

L38 ANSWER 25 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1986-089051 [14] WPIX
DNN N1986-065139 DNC C1986-037863

TI Capacitive devices, esp. for filtered connectors - comprise conductive substrate carrying laminated, heat-bonded and sintered capacitor structures.
DC L03 U25 V01 V04 W02
IN BLAZE, D C
PA (ALLC) ALLIED CORP
CYC 7
PI EP 175988 A 19860402 (198614)* EN 22p
R: DE FR GB IT
JP 61113221 A 19860531 (198628)
US 4733328 A 19880322 (198815)
CA 1259677 A 19890919 (198943)
ADT JP 61113221 A JP 1985-206758 19850920; US 4733328 A US 1986-943526 19861218
PRAI US 1984-653252 19840924; US 1986-943526 19861218
AB EP 175988 A UPAB: 19930922
Capacitive element comprises a substrate carrying laminated structures, each consisting of: a non-conductive, finely divided, sintered layer heat-bonded to the substrate; and a metallic conductive, finely divided, sintered layer heat-bonded to the non-conductive layer. Pref. the substrate is Cu, **non-conductive** material is **ceramic**; and conductive metal is Cu.
Ceramic is an oxide material, ferro-electric material, synthetic ceramic or glass, esp. a ferro-electric opt. mixed with one or more glasses. Non-conductive layer thickness is 0.020-0.10 mm; conductive layer thickness is 0.005-0.075 mm.
USE/ADVANTAGE - In a filtered connector (claimed). Devices can be formed in automated processes with good yield, of thin dimension and with good reliability.
1/2

L38 ANSWER 26 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1982-G4251E [22] WPIX
TI Optical transducer for measuring angular position of shaft - has photocells connected to film resistors preset to design values by selective burning using laser.
DC W05
IN CONTA, R
PA (OLIT) OLIVETTI & CO SPA
CYC 4
PI GB 2088048 A 19820603 (198222)* 7p
DE 3145833 A 19820624 (198226)
US 4393591 A 19830719 (198331)
GB 2088048 B 19840718 (198429)
IT 1129862 B 19860611 (198745)
DE 3145833 C 19920409 (199215) 7p
ADT GB 2088048 A GB 1981-34430 19811116
PRAI IT 1980-68755 19801117
AB GB 2088048 A UPAB: 19930915
The optical transducer for determining the angular position of a rotating member relative to a fixed structure, comprises a notched disc (13) rotatable inside a support housing (12), a light emitter (18) and photovoltaic cells (19) for detecting the passage of light through the disc notches. The active and passive elements of an **electronic circuit** connected to the photovoltaic cells are carried by a single ceramic plate (21), which also acts as a support for the cells (19). The circuit comprises trimming resistors in the form of films deposited on the ceramic plate and connected to the amplifiers by the photovoltaic cells and the ceramic plate also carries a conductor having a microsection which defines an edge reference point.
In order for the signals generated by the amplifiers to have

constant, predetermined peak values, the values of the resistors are trimmed during the production stage by means of a laser which selectively burns away parts of the resistors. The ceramic plate (21) is cemented on to the transducer housing (12), which is then positioned on the laser appts. The operations involved in presetting the resistors is carried out with the transducer in operation, and the laser need only be focused and pre-positioned (at the edge reference point) once for the entire circuit. 2

L38 ANSWER 27 OF 27 WPIX (C) 2003 THOMSON DERWENT
AN 1981-J3129D [36] WPIX
TI Electrical battery economiser circuit - has encapsulated circuit with Zener diode, current limiting bias resistor and high-gain germanium output transistors.
DC U24 X16
PA (EVAN-I) EVANS V S
CYC 1
PI GB 2070294 A 19810903 (198136)* 5p
GB 2070294 B 19840418 (198416)
ADT GB 2070294 A GB 1980-5564 19800219
PRAI GB 1980-5564 19800219
AB GB 2070294 A UPAB: 19930915
The device is for improving performance of a battery supplying a load, e.g. transistor radios that will operate at a voltage below nominal output of the battery. It has an encapsulated **electronic circuit** preferably comprised of a Zener diode (16), current limiting bias resistor (14), and complementary high-grain germanium output transistors (TR1,2), with a very low leakage current measured in microamps. Connectors to the battery and load can conveniently have press-stud elements.

The device may be mounted in a body fitting to a vehicle lighter socket with connections between the device and contacts of the body. The output leads carry press-stud elements to **connect** **electrical** wiring of the product. The input leads also carry press-stud elements to **connect** to an **electrical** battery.

01/06/2003

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01/06/2003

Set	Items	Description
S1	112096	ELECTR?(W)(APPARATUS OR DEVICE? OR CIRCUIT?)
S2	791	RESISTIVE(2N)CONDUCTIV?
S3	25649	ELECTRIC?(2N)(CONNECT? OR JOIN? OR BOND?)
S4	756	FR4 OR FLAME(W)RETARDANT(W)(4 OR FOUR OR IV)
S5	17762	(MOTHER OR CIRCUIT?)(W)(BOARD) OR MOTHERBOARD? OR CIRCUITBOARD?
S6	89	NON(W)CONDUCT?(2N)CERAMIC? OR NONCONDUCT?(2N) CERAMIC?
S7	5501	PASSIVE(W)COMPONENT?
S8	0	AU=(GALVAGNI J L OR GALVAGNI, J L OR GALVAGNI, JOHN L OR GALVAGNI JOHN L)
S9	4	AU=(GALVAGNI J OR GALVAGNI, J OR GALVAGNI, JOHN OR GALVAGNI JOHN)
S10	77	S5 AND S4
S11	62	RD (unique items)
S12	0	S5 AND S6
S13	2	S5 AND S2
S14	119	S5 AND S7
S15	20	S14 AND (MULTILAYER? OR MULTI(W)LAYER?)
S16	2	S5 AND S2
S17	22	(S13 OR S15 OR S16) NOT S10
S18	20	RD (unique items)
S19	6	S1 AND S4
S20	8	S1 AND S2
S21	2	S1 AND S6
S22	0	S1 AND S9
S23	159	S1 AND S7
S24	4	S23 AND VIA
S25	18	S23 AND (MULTILAYER? OR MULTI(W)LAYER?)
S26	19	S23 AND (STACKED OR MOUNT?)
S27	46	(S19:S21 OR S24:S26) NOT (S17 OR S10)
S28	44	RD (unique items)
S29	90	(S14 OR S23) AND RESISTOR? ?
S30	0	(S14 OR S23) AND RESISTOR? ? AND CAPACITOR? ? AND VARISTOR? ? AND THERMISTORS
S31	102	(S14 OR S23) AND CAPACITOR? ?
S32	1	(S14 OR S23) AND VARISTOR? ?
S33	4	(S14 OR S23) AND THERMISTOR? ?
S34	3	(S32 OR S33) NOT (S19:S21 OR S24:S26 OR S17 OR S10)
S35	3	RD (unique items)
S36	76	S31 NOT (S32 OR S33 OR S19:S21 OR S24:S26 OR S17 OR S10)
S37	72	RD (unique items)
S38	9	S37 AND (STACKED OR MOUNT?)
S39	1	S37 AND STACK?
S40	10	S38 OR S39

01/06/2003

9/3,AB/1 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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00635812 Genuine Article#: EH372 Number of References: 16
Title: ELECTROSTRICTIVE ACTUATORS AND THEIR USE IN OPTICAL APPLICATIONS
Author(s): **GALVAGNI J**
Corporate Source: AVX CERAM CORP,CORP RES LABS,POB 867/MYRTLE BEACH//SC/29577
Journal: OPTICAL ENGINEERING, 1990, V29, N11, P1389-1391
Language: ENGLISH Document Type: ARTICLE

9/3,AB/2 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs
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0938138 H.W. WILSON RECORD NUMBER: BAST91002326
Electrostrictive actuators and their use in optical applications
Galvagni, John;
Optical Engineering v. 29 (Nov. '90) p. 1389-91
DOCUMENT TYPE: Feature Article ISSN: 0091-3286

9/3,AB/3 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
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15591517 PASCAL No.: 02-0293250
Controlling capacitor parasitics for high frequency decoupling
Microelectronics : Baltimore MD, 9-11 October 2001
KORONY George; RITTER Andrew; GONZALEZ-TITMAN Carlos; HOCK Joseph; **GALVAGNI John**; HEISTAND Robert II
AVX Corporation, 2200 AVX Drive, Myrtle Beach, SC 29577, United States
International Society for Optical Engineering, Bellingham WA, United States
International symposium on microelectronics (Baltimore MD USA) 2001-10-09
Journal: SPIE proceedings series, 2001, 4587 605-609
Language: English
The need of decoupling power planes at ever-higher frequencies drives the design and production of very low inductance and controlled series resistance capacitors. The loop impedance model, usually applied to the board design, can also help in designing new low inductance high frequency decoupling capacitors. The capacitor structures with current-cancellation and array termination have an approximate three order of magnitude lower inductance than the usual MLCs. The testing of such low inductance capacitors is not a trivial question and needs carefully designed test boards and measuring methods.

9/3,AB/4 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal
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10494636 PASCAL No.: 93-0003887
Electrostrictive actuators and their use in optical applications
GALVAGNI J
AVX Corp. , Corp. Research Labs, Myrtle Beach SC 29577, USA

Journal: Optical engineering, 1990, 29 (11) 1389-1391
Language: English

01/06/2003

11/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7394974 INSPEC Abstract Number: B2002-11-2210D-014
Title: Method to evaluate the electrical performance of printed **circuit board** laminate materials
Author(s): Watkins, M.J.
Author Affiliation: Motorola Inc., Fort Lauderdale, FL, USA
Conference Title: 52nd Electronic Components and Technology Conference 2002. (Cat. No.02CH37345) p.1539-47
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA xxxiv+1789 pp.
ISBN: 0 7803 7430 4 Material Identity Number: XX-2002-01381
U.S. Copyright Clearance Center Code: 0-7803-7430-4/02/$17.00
Conference Title: Proceedings of 52nd Electronic Components and Technology Conference
Conference Sponsor: IEEE Components, Packaging, & Manuf. Technol. Soc.; Electronic Components, Assemblies & Mater. Assoc
Conference Date: 28-31 May 2002 Conference Location: San Diego, CA, USA
Language: English
Abstract: Board materials are rapidly changing to meet the requirements for low cost, environmentally preferred, and data rate (3G) applications. Therefore, it is necessary to have electrical test and characterization methods that are quick, accurate, and able to be implemented during development, design, and manufacture. In order to meet these needs, a characterization method was developed based on RF resonator filter printed circuit structures. The method is repeatable, cost effective, and uses automated test equipment and procedures. The design of the filter structures is such that the sensitivity is capable of detecting critical RF attributes of the dielectric material and the printed circuit manufacturing process. The test procedure is capable of determining variation in dielectric constant, material loss, dielectric thickness, and layer-to-layer alignment. The results are given in terms relevant to circuit design applications - selectivity, bandwidth, and insertion loss. This paper discusses the electrical performance of printed **circuit board** dielectrics needed to meet today's requirements, the novel test method used to evaluate the dielectric and manufacturing process, and the data collected for materials such as **FR4**, environmentally preferred, and low Dk high performance laminates using the new test method.
Subfile: B

11/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7371637 INSPEC Abstract Number: B2002-10-2210B-003
Title: Special processing needs for thermally-sensitive designs
Author(s): Lynch, J.; Sommervold, D.
Author Affiliation: Autosplice Inc., San Diego, CA, USA
Journal: Surface Mount Technology vol.16, no.6 p.34-40
Publisher: PennWell Publishing,
Publication Date: June 2002 Country of Publication: USA
CODEN: SMTEEL ISSN: 0893-3588
SICI: 0893-3588(200206)16:6L.34:SPNT;1-5
Material Identity Number: N547-2002-008
Language: English

Abstract: Thermal management challenges have become increasingly important across a widening range of applications for the basic reason that "watt-density" requirements of many products have escalated well beyond the capabilities of conventional **FR4**-based printed **circuit board** (PCB) designs. Advanced thermal management techniques initially came into prominence within power-control and conversion applications in which critical design parameters required packing high-wattage functions into compact devices. For such use, it is vital to minimize the risk of thermal damage to internal circuitry and surrounding components in the final assembly.
Subfile: B

11/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

7365706 INSPEC Abstract Number: B2002-10-1350-007
Title: Thick metal plate insertion make **FR4** multilayer board a simple carrier for RF power circuits
Author(s): Buoli, C.; Biffi, G.; Turillo, T.; Zingirian, A.
Author Affiliation: Siemens Inf. & Cornmunication Networks S.p.A., Milan, Italy
Conference Title: 31st European Microwave Conference 2001. Conference Proceedings Part vol.1 p.157-60 vol.1
Publisher: Microwave Eng. Europe, London, UK
Publication Date: 2001 Country of Publication: UK 3 vol.(456+304+486) pp.
Material Identity Number: XX-2001-01675
Conference Title: Proceedings of 31st European Microwave Conference
Conference Date: 24-28 Sept. 2001 Conference Location: London, UK
Language: English
Abstract: In order to reduce the size and cost of microwave circuits and to simplify their integration with IF, control and power supply networks, we tested a simple solution that allows **FR4** boards to be used also for microwave circuits. Since **FR4** boards are necessarily present in every piece of equipment for power supplies, control, digital and IF circuits, it becomes possible to reduce the number of boards or modules, collecting all the networks (operating from DC to tenths of Gigahertz) together on the same **FR4** multilayer board. The typical RF requirements of good thermal and electrical grounding, and the need for a carrier for "chip on board" monolithic assembly, are all achieved through the insertion of a copper plate a few tenths of a millimetre thick. This copper plate replaces the second metal layer of the **FR4** multilayer while remaining within the standard **FR4** process; monolithics can be mounted on it simply by opening a window on the first layer.
Subfile: B

11/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

7356666 INSPEC Abstract Number: B2002-10-2210D-003
Title: A universal printed **circuit-board** surface for ultrasonic and thermosonic wire bonding with regard to COB-technology
Author(s): Schneider-Ramelow, M.; Lang, K.-D.; Rudolf, F.
Journal: VTE Aufbau- und Verbindungstechnik in der Elektronik no.3 p.E46-50

Publisher: Verlag fur Schweissen und Verwandte Verfahren DVS-Verlag,
Publication Date: June 2002 Country of Publication: Germany
CODEN: VTEVFC ISSN: 0946-7777
SICI: 0946-7777(200206)3L.e46:UPCB;1-W
Material Identity Number: G388-2002-004
Language: English
Abstract: The bondability and reliability of Au and AlSi standard wires on **FR4** printed circuit-boards with Cu/Ni/Pd/flash Au metallisations were examined in the context of a BMBF-sponsored composite project to explore the use of microsystems in the rough and humid environment of marine biology. This served to establish the good bondability of the finish metallisation for both wires and wire bonding processes. The connections on the boundary zone between the wire and the substrate metallisation were generated facing the Pd. Both systems (Au/Pd and Al/Pd) proved to be stable in pull tests after having been exposed to 150 degrees C for up to 2000 h and to 2000 cycles of temperature shock treatment (-40 degrees C/125 degrees C), i.e. neither pull lift-offs nor values below the required minimum strength levels were observed.
Subfile: B

11/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

7312490 INSPEC Abstract Number: B2002-08-5270B-023
Title: Small printed integrated inverted-F antenna for Bluetooth application
Author(s): Ali, M.; Hayes, G.J.
Author Affiliation: Dept. of Electr. Eng., South Carolina Univ., Columbia, SC, USA
Journal: Microwave and Optical Technology Letters vol.33, no.5 p. 347-9
Publisher: Wiley,
Publication Date: 5 June 2002 Country of Publication: USA
CODEN: MOTLEO ISSN: 0895-2477
SICI: 0895-2477(20020605)33:5L.347:SPII;1-0
Material Identity Number: M687-2002-009
Language: English
Abstract: A printed integrated inverted-F antenna is introduced which operates in the Bluetooth frequency band (2.4-2.485 GHz). The proposed antenna is a part of the radio frequency printed **circuit board** (PCB) of a cellular telephone or a personal digital assistant (PDA). The antenna being an integral part of the PCB reduces the cost and complexity of designing and manufacturing a separate antenna. The maximum dimension of the antenna on standard **FR4** substrate is 25*5*1 mm/sup 3/. The antenna operates within 2:1 voltage standing wave ratio (VSWR) and has a free-space peak gain of 1.5 dBi.
Subfile: B

11/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

7068572 INSPEC Abstract Number: B2001-11-0170J-267
Title: CBGA to **FR4** printed **circuit board** with no underfill thermal mismatch study
Author(s): Howieson, M.

Author Affiliation: Thin Film Technol., North Mankato, MN, USA
Conference Title: 2001 Proceedings. 51st Electronic Components and Technology Conference (Cat. No.01CH37220) p.1487-95
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA xxxiii+1518 pp.
ISBN: 0 7803 7038 4 Material Identity Number: XX-2001-01138
U.S. Copyright Clearance Center Code: 0 7803 7038 4/2001/$10.00
Conference Title: 51st Electronic Components and Technology Conference 2001. Proceedings
Conference Sponsor: Components, Packaging, & Manuf. Technol. (CPMT) Soc. IEEE; Electron. Components Assemblies & Mater. Assoc. (ECA); Electron. Components Sector of the Electron. Ind. Alliance
Conference Date: 29 May-1 June 2001 Conference Location: Orlando, FL, USA
Language: English
Abstract: With the turn of the century, BGA-type packages are now widely used in the microelectronic industry. From a passive component manufacture that uses ceramic (alumina) as its main substrate carrier, the reliability of ceramic BGA (CBGA) packages mounted to **FR4** printed **circuit board** is still a noteworthy concern. The reliability concern is for the different thermal expansion rates of the two substrate materials and how that CTE mismatch creates added stress on the BGA solder joint when thermal cycled. The point of thermal fatigue in a solder joint is an important factor of CBGA packages and knowing how many thermal cycles can be run before failure in the solder BGA joint is a must for designing a reliable CBGA package. In this paper, we describe a reliable, quick, FEA method to accurately predict the number of thermal fatigue cycles to produce a crack failure in the CBGA solder joint.
Subfile: B

11/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

6966727 INSPEC Abstract Number: B2001-08-2210D-002
Title: Evaluation and implementation of halogen-free printed **circuit board** materials for telecom applications
Author(s): Valfridsson, M.
Journal: CircuiTree vol.13, no.11 p.116, 118, 120
Publisher: Business News Publishing Co,
Publication Date: Nov. 2000 Country of Publication: USA
CODEN: CIRCF6 ISSN: 1059-843X
SICI: 1059-843X(200011)13:11L.116:EIHF;1-1
Material Identity Number: E342-2001-002
Language: English
Abstract: Halogen-free flame-retardant materials are more environmentally friendly than **FR4**/FR5 for printed **circuit board** processing. Assembly, using lead-free solders as well as regular eutectic Sn/Pb solders, shows satisfying results. The electrical characteristics of the materials differ to those of **FR4**/FR5, which makes the material selection process for some applications difficult.
Subfile: B

11/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

6899775 INSPEC Abstract Number: B2001-05-0520J-035
Title: Electroless nickel plating bath composition and replenishment for microvia plating processes
Author(s): Stoukatch, S.; Zhang, S.; Vanfleteren, J.; Vereeken, M.; Van Calster, A.; Vandecasteele, B.
Author Affiliation: ELIS/TFCG-IMEC, Ghent Univ., Belgium
Conference Title: IMAPS - EUROPE PRAGUE 2000. European Microelectronics Packaging and Interconnection Symposium. Proceedings p.447-52
Editor(s): Mach, P.; Urbanek, J.
Publisher: IMAPS-Int. Microelectron. & Packaging Soc, Prague, Czech Republic
Publication Date: 2000 Country of Publication: Czech Republic xx+500 pp.
ISBN: 80 238 5509 3 Material Identity Number: XX-2000-01483
Conference Title: Proceedings of IMAPS Europe Prague 2000
Conference Date: 18-20 June 2000 Conference Location: Prague, Czech Republic
Language: English
Abstract: Low cost electroless nickel/gold (Ni/Au) surface finishes for package I/Os and **circuit board** features are becoming increasingly popular. The plating process developed here was applied for electroless plating of Ni/Au on micropads on a fine-line **FR4** PCB. On top of copper, a 20 mu m thick photoimageable dielectric is applied and patterned. This process allows us to plate PCBs characterized by a wide range of feature dimensions, varying from micropads (<100 mu m) to relatively large sizes of several square mm. Using monitoring and replenishment procedures, consistent plating of subsequent batches of PCBs was executed until a 1 time turnover of the bath was reached.
Subfile: B

11/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

6866421 INSPEC Abstract Number: B2001-04-8360-186
Title: The effect of printed **circuit board** on cooling and EMC of switched mode power supply
Author(s): Sippola, M.; Von Rauner, T.; Siren, H.
Author Affiliation: Appl. Electron. Lab., Helsinki Univ. of Technol., Espoo, Finland
Conference Title: 2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018) Part vol.3 p. 1267-72 vol.3
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 3 vol. xxv+1662 pp.
ISBN: 0 7803 5692 6 Material Identity Number: XX-2000-02335
U.S. Copyright Clearance Center Code: 0 7803 5692 6/2000/$10.00
Conference Title: Proceedings of the 2000 Power Electronics Specialist Conference
Conference Date: 18-23 June 2000 Conference Location: Galway, Ireland
Language: English
Abstract: EMC and thermal properties of seven **FR4**, FLEX and IMS based printed circuit boards (PCB) were studied experimentally with a boost type switched mode power supply. Thermal performance of PCBs was measured using a DPACK transistor as test load with boards mounted into metal enclosure. Conducted emissions (150 kHz-30 MHz) were divided into differential and common mode components. For EMI measurements from 30 MHz to 1 GHz an absorbing clamp was used. Thermal resistance of test cases

varied from 58.7 degrees K/W of 1-layer **FR4** to 7.9 degrees K/W of 2-layer INIS. The total common mode noise energy of worst ease (1-layer FLEX) was 58.5 times higher than with the best (2-layer IMS). The prices of PCBs in the study varied from 0.38$ (layer **FR4**) to 2.15$ (2-layer IMS).

Subfile: B

11/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

6762685 INSPEC Abstract Number: B2000-12-2210B-012

Title: Using experimental analysis to evaluate the influence of printed **circuit board** construction on the thermal performance of four package types in both natural and forced convection

Author(s): Lohan, J.; Tiilikka, P.; Rodgers, P.; Fager, C.-M.; Rantala, J.

Author Affiliation: Mech. & Ind. Eng. Dept., Galway-Mayo Inst. of Technol., Ireland

Conference Title: ITHERM 2000. The Seventh Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (Cat. No.00CH37069) Part vol. 2 p.213-25 vol. 2

Editor(s): Kromann, G.B.; Culham, J.R.; Ramakrishna, K.

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2000 Country of Publication: USA 2 vol. (xiii+viii+819) pp.

ISBN: 0 7803 5912 7 Material Identity Number: XX-2000-01811

U.S. Copyright Clearance Center Code: 0 7803 5912 7/2000/$10.00

Conference Title: ITHERM 2000. The Seventh Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems

Conference Sponsor: CPMT/IEEE

Conference Date: 23-26 May 2000 Conference Location: Las Vegas, NV, USA

Language: English

Abstract: As the functionality of electronic systems increase, so does the complexity of printed **circuit board** (PCB) design, with greater component packing densities requiring additional internal signal, power and ground layers to facilitate interconnection. The extra copper content introduced increases PCB thermal conductivity and heat spreading capability, which can strongly influence component operating temperature. Therefore, this experimental study sought to quantify the impact of PCB construction on component operating temperature and relate this sensitivity to the package design, PCB effective conductivity and convective environment. This was achieved by measuring the steady state thermal performance of four package types (PSO20: heat slug up, PSO20: heat slug down, LFBGA80 and SBGA352) on up to six different, single-component thermal test PCBs in the standard natural and forced convection environments. Test velocities ranged from 0.5 m/s to 5.0 m/s and all test components contained a thermal test die. Measurements of junction temperature and component-PCB surface temperature distributions are both presented for power dissipation levels within the range 0.5 to 6.0 Watts. The study includes the low and high conductivity JEDEC standard, **FR4**-based test PCBs and typical application boards. As each PCB had a different internal structure and effective thermal conductivity, this study highlights the sensitivity of component operating temperature to the PCB, provides benchmark data for validating numerical models, and helps one assess the applicability of standard junction-to-air thermal resistance (theta /sub JA/ and theta /sub JMA/), as well as both junction-to-board (Psi /sub JB/) and junction-to-top (Psi /sub JT/) thermal characterisation parameters for

design purposes on nonstandard PCBs.
Subfile: B
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11/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

6724587 INSPEC Abstract Number: B2000-11-2210B-002
Title: Experimental and numerical investigation into the influence of printed **circuit board** construction on component operating temperature in natural convection
Author(s): Lohan, J.; Tiilikka, P.; Rodgers, P.; Fager, C.-M.; Rantala, J.
Author Affiliation: Dept. of Mech. & Ind. Eng., Galway-Mayo Inst. of Technol., Galway, UK
Journal: IEEE Transactions on Components and Packaging Technologies vol.23, no.3 p.578-86
Publisher: IEEE,
Publication Date: Sept. 2000 Country of Publication: USA
CODEN: ITCPFB ISSN: 1521-3331
SICI: 1521-3331(200009)23:3L.578:ENII;1-I
Material Identity Number: H324-2000-004
U.S. Copyright Clearance Center Code: 1521-3331/2000/$10.00
Language: English
Abstract: The steady state thermal performance of an isolated SO-8 package is experimentally characterized on five thermal test printed circuit boards (PCBs) and the results compared against corresponding numerical predictions. The study includes the low and high conductivity JEDEC standard, **FR4** test PCBs and typical application boards. With each PCB displaying a different internal structure and effective thermal conductivity, this study highlights the sensitivity of component operating temperature to the PCB, provides benchmark data for validating PCB numerical modeling methodologies, and helps one assess the applicability of standard junction-to-ambient thermal resistance (theta /sub JA/) data for design purposes on nonstandard PCBs. Measurements of junction temperature and component-PCB surface temperature distributions were used to identify the most appropriate modeling methodology for both the component and the PCB. Based on these results, a new PCB modeling methodology is proposed that conserves the need for modeling detail without compromising prediction accuracy.
Subfile: B

11/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

6724586 INSPEC Abstract Number: B2000-11-2210B-001
Title: A benchmark study of computational fluid dynamics predictive accuracy for component-printed **circuit board** heat transfer
Author(s): Eveloy, V.; Lohan, J.; Rodgers, P.
Author Affiliation: Dept. of Mech. & Aeronaut. Eng., Limerick Univ., Ireland
Journal: IEEE Transactions on Components and Packaging Technologies vol.23, no.3 p.568-77
Publisher: IEEE,
Publication Date: Sept. 2000 Country of Publication: USA
CODEN: ITCPFB ISSN: 1521-3331

SICI: 1521-3331(200009)23:3L.568:BSCF;1-7
Material Identity Number: H324-2000-004
U.S. Copyright Clearance Center Code: 1521-3331/2000/$10.00
Language: English
Abstract: The application of computational fluid dynamics (CFD) analysis for the thermal design of electronic systems has the potential to enable accurate solutions to be generated and quickly assessed. With the use of validated numerical models, numerical analysis can also be used to provide useful insights into heat transfer processes which could otherwise be difficult to characterize experimentally. However, the capabilities of the CFD tool need to be carefully evaluated so as to provide a degree of confidence in prediction accuracy, thereby minimizing the need to qualify thermal designs. Such an evaluation is presented in this paper, which represents the culmination of a benchmark study by Rodgers et al. [1999]. This overall study assesses the predictive accuracy of a commercial CFD code for both natural and forced convection heat transfer of single- and multicomponent printed circuit boards (PCBs). Benchmark criteria were based on both component junction temperature and component-PCB surface temperature profiles. In the context of the overall study, this paper brings these analyses together to provide a more comprehensive assessment of CFD predictive accuracy for component junction temperature. Additionally the validated numerical models are used to further investigate the sensitivity of component heat transfer to convective environment, both natural and forced, component position relative to the PCBs leading edge, impact of upstream aerodynamic disturbance, and the representation of PCB FR4 thermal conductivity. The significance of the listed variables is quantified by analyzing predicted component energy balances. Qualitative descriptions of the fluid flow fields obtained using a novel paint film evaporation technique are also provided in this study. Both analyses yield new insights of the heat transfer processes involved and sources of numerical error.
Subfile: B

11/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

6715199 INSPEC Abstract Number: B2000-11-2560R-009
Title: MOSFET BGA package
Author(s): Joshi, R.; Granada, H.; Tangpuz, C.
Author Affiliation: Fairchild Semicond. Corp., Sunnyvale, CA, USA
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070) p.944-7
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xxxv+1756 pp.
ISBN: 0 7803 5908 9 Material Identity Number: XX-2000-01366
U.S. Copyright Clearance Center Code: 0 7803 5908 9/2000/$10.00
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, and Manuf. Technol. Soc. of IEEE; Electronic Ind. Alliance
Conference Date: 21-24 May 2000 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: The trend towards miniaturization in electronics is the main driver for small form factor packages. The industry has taken various evolutionary steps towards this objective: Small Outline Integrated Circuit (SOIC) to Thin Shrink Small Outline Packages (TSSOP), Quad Flat Packs (QFP) to Thin Quad Flat Packs (TQFP). Typical Chip/Package area ratios for

SOJ/TSOP packages have been reported in the range of 40%. An ultimate goal would be to develop a package which would be the size of the die itself. Flip Chip also known in the industry as IBM's C-4 technology can be considered to be an early example of a die sized package where the chip is directly attached to a substrate using solder bumps. This technology had some difficulties which limited its implementation: it could not be used easily on **FR4** boards without a special underfill process (this was needed to minimize stress issues due to coefficient of expansion mismatch between die and printed **circuit board** substrates). Other issues centered around testing, handling and shipping of bare die. Even today, there are few vendors of Known Good Die (KGD). Contract manufacturing offering flip chip assembly is also limited.
Subfile: B

11/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

6709710 INSPEC Abstract Number: B2000-10-2210D-034
Title: Electro-optical printed **circuit board** (EOPCB)
Author(s): Schmieder, K.; Wolter, K.-J.
Author Affiliation: Electron. Technol. Lab., Tech. Univ. Dresden, Germany
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070) p.749-53
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xxxv+1756 pp.
ISBN: 0 7803 5908 9 Material Identity Number: XX-2000-01366
U.S. Copyright Clearance Center Code: 0 7803 5908 9/2000/$10.00
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, and Manuf. Technol. Soc. of IEEE; Electronic Ind. Alliance
Conference Date: 21-24 May 2000 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: Recently attention has been given to optical waveguides in order to elude the interconnect bottleneck caused by insufficient discrete copper wiring at the board-level. But the cost increase, due to additional manufacturing steps and equipment, are justifiable only for those applications where electronic interconnections are unable to perform satisfactorily. That's why the future high-performance board will most likely be a hybrid carrier which combines electrical and optical circuitry. This paper will introduce a suitable technology to generate multimode waveguides on standard base materials like **FR4**. Great importance has been attached to designing a manufacturing process for the optical layer, which is essentially compatible with conventional PCB production. The results of early characterizations encouraged us to pursue this technology. Our layout contains bent waveguides, optical bifurcations and even crosses, the latter being unthinkable in electrical wiring layout. We will also address concerns like sidewall roughness of the waveguide structures, propagation loss, thermal and environmental stability, etc. which all are significant to the high performance EOPCB.
Subfile: B

11/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

01/06/2003

6493763 INSPEC Abstract Number: B2000-03-0170J-176
Title: Surface graft copolymerization enhanced lamination of poly(tetrafluoroethylene) film to copper and epoxy-based print **circuit board** (PCB)
Author(s): Zhang, J.; Cui, C.Q.; Lim, T.B.; Kang, E.T.
Author Affiliation: Adv. Packaging Dev. Support, Inst. of Microelectron., Singapore
Journal: Transactions of the ASME. Journal of Electronic Packaging vol.121, no.4 p.291-6
Publisher: ASME,
Publication Date: Dec. 1999 Country of Publication: USA
CODEN: JEPAE4 ISSN: 1043-7398
SICI: 1043-7398(199912)121:4L.291:SGCE;1-O
Material Identity Number: N602-2000-001
Language: English
Abstract: Lamination of poly(tetrafluoroethylene) (PTFE) film to a copper foil or to an epoxy-based PCB substrate (**FR4**/sup (R)/) was carried out. Lamination was achieved during surface graft copolymerization of glycidyl methacrylate (GMA) on an Ar plasma pretreated PTFE film at elevated temperature in the presence of an epoxy resin adhesive. The plasma pretreatment introduces peroxides which are thermally degraded into free radicals to initiate the graft polymerization of GMA on the PTFE surface. The graft copolymerization with concurrent lamination is carried out in the absence of a polymerization initiator or system degassing. The modified surfaces and interfaces are characterized by X-ray photoelectron spectroscopy (XPS) and atomic force microscopy (AFM). The adhesion strength between the PTFE film and copper or the **FR4**/sup (R)/ substrate was assessed by the T-peel strength test method. The adhesion strength was affected by plasma pretreatment time, as well as the grafting and curing temperature. The PTFE/GMA-epoxy resin/Cu and PTFE/GMA-epoxy resin/**FR4** assemblies exhibit significant higher interfacial adhesion strengths compared to those assemblies in which only epoxy resin or GMA was used. They also exhibit better interfacial adhesion reliability. The PTFE/GMA-epoxy resin/Cu and PTFE/GMA-epoxy resin/**FR4**/sup (R)/ joints delaminated by cohesive failure inside the bulk of PTFE film. The results suggest that the enhanced adhesion between the graft-modified PTFE film and Cu or **FR4** /sup (R)/ surfaces is attributable to the formation of covalent bonds between the tethered GMA graft chains on PTFE and the epoxy resin network.
Subfile: B

11/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

6467282 INSPEC Abstract Number: B2000-02-0170E-027
Title: Low-cost high-performance DC plus RF accelerated life-test system
Author(s): Whitefield, D.; Khanna, R.
Author Affiliation: Alpha Ind., Woburn, MA, USA
Conference Title: 1998 GaAs Reliability Workshop. Proceedings (Cat. No.98EX219) p.14-18
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1998 Country of Publication: USA vii+105 pp.
ISBN: 0 7908 0065 9 Material Identity Number: XX-1999-01408
U.S. Copyright Clearance Center Code: 0 7908 0065 9/98/$10.00
Conference Title: 1998 GaAs Reliability Workshop. Proceedings
Conference Sponsor: JEDEC JC-14.7 Committee on Gallium Arsenide Reliability and Quality Standards

Conference Date: 1 Nov. 1998 Conference Location: Atlanta, GA, USA
Language: English
Abstract: A novel design has been developed for an elevated-temperature RF life-test system which has achieved the goals of maintaining a low cost, a high degree of flexibility and a high level of system reliability. The design uses simple techniques to achieve a baseplate temperature of up to 250 degrees C for the packaged device under test (DUT) while the RF and DC circuitry remains cool at less than 65 degrees C. An **FR4** printed **circuit board** is utilized for combining the DC bias and the 2 GHz RF signal, and allows easy modification for RF matching, oscillation suppression, and DC biasing options. Each DUT has its own temperature controller and its own DC voltage supplies, which allow each of the 16 DUTs to have different operating conditions if needed. All units are driven by the same RF source which is split 16 ways and can deliver up to 0.5 W to each DUT.
Subfile: B

11/3,AB/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

6455650 INSPEC Abstract Number: B2000-02-2210D-027
Title: A two-layer high density printed **circuit board** and its reliability
Author(s): Zhang, S.; De Baets, J.; Van Calster, A.
Author Affiliation: ELIS/TFCG, IMEC, Ghent, Belgium
Journal: Microelectronics Reliability vol.39, no.9 p.1337-41
Publisher: Elsevier,
Publication Date: Sept. 1999 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
SICI: 0026-2714(199909)39:9L.1337:LHDP;1-Q
Material Identity Number: G489-1999-008
U.S. Copyright Clearance Center Code: 0026-2714/99/$20.00
Language: English
Abstract: The fabrication and reliability of a two-layer high density PCB test vehicle are reported in this paper. The test board consisted of two copper layers that were sequentially built up on one side of a **FR4** substrate and interconnected through a photovia dielectric layer. Various test structures were fabricated for reliability testing. Thermal cycling, 85 degrees C/85%RH ageing, and multiple reflow excursions were performed to test the reliability of electrical continuity and insulation. Peel strength was measured after fabrication as well as after 150 degrees C annealing and reflow excursions. Initial results have revealed that photovias may be more reliable than conventional through vias.
Subfile: B

11/3,AB/18 (Item 18 from file: 2)
DIALOG(R)File 2:INSPEC

6399166 INSPEC Abstract Number: B1999-12-0170J-096
Title: Environmental effects in component packaging selection
Author(s): Siddhaye, S.; Sheng, P.; Ooi, C.
Author Affiliation: California Univ., Berkeley, CA, USA
Journal: IEEE Transactions on Electronics Packaging Manufacturing vol.22, no.3 p.185-90
Publisher: IEEE,

Publication Date: July 1999 Country of Publication: USA
CODEN: ITEPFL ISSN: 1521-334X
SICI: 1521-334X(199907)22:3L.185:EECP;1-5
Material Identity Number: H313-1999-003
U.S. Copyright Clearance Center Code: 1521-334X/99/$10.00
Language: English

Abstract: Design for environment activities in electronics have been focused on issues of product life-cycle at the board design level and to facility-level process and material choices at the semiconductor fabrication level. An important bridge between these two domains has been the influence of component selection, particularly packaging selection, on environmental impacts. Component packaging influences waste generation in two respects. First, packaging type (i.e. DIP, QFP, BGA, etc.) and size dictates direct production waste in stamping, molding and plating operations. The waste streams from these operations include copper, polymerized thermoset plastic, caustic and acidic effluents and also small traces of silver epoxy. Since many waste components are nonrecyclable and/or have high hazardous content, effective management of direct waste emissions is a critical design task. Second, packaging selection indirectly affects waste generation at the printed **circuit board** (PCB) level through layout and board sizing decisions. The waste streams from board fabrication include composite scrap (usually glass epoxy), metals (copper foil and dissolved solutions) and catalyst wastes (aqueous photoresist, developer and stripper solutions and hole drilling scrap and tooling). The analysis approach undertaken in this study relies on the development of a toolset of unit process models for packaging manufacturing which develops relationships between package parameters, process parameters and waste outputs. By linking a chain of process models, a mathematical description of a packaging production sequence can be estimated. The models are formulated using the line data collected on plastic quad flat package (PQFP) lines. From the process models, a case comparison of the environmental impacts for two alternative packages for components is developed. Two designs, a design that employs almost all small outline integrated circuits (SOICs) and dual in-line packages (DIPs) (except where lead count necessitates PQFPs) vs. the same design that employs all PQFPs are considered. A case study illustrating the corresponding PCB level impacts due to component packaging selection is also presented. The bare board chosen in both cases is a standard **FR4** board.

Subfile: B

11/3,AB/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC

6266241 INSPEC Abstract Number: B1999-07-0170J-129, C1999-07-7410D-083
Title: A CAE approach for the thermal design of compact electronic enclosures. A laptop computer case study
Author(s): Ali, I.A.
Author Affiliation: Flomerics Inc., Marlborough, MA, USA
Conference Title: Advances in Electronic Packaging 1997. Proceedings of the Pacific Rim/ASME International Intersociety Electronic and Photonic Packaging Conference. INTERpack '97 Part vol.2 p.2131-6 vol.2
Editor(s): Suhir, E.; Shiratori, M.; Lee, Y.C.; Subbarayan, G.
Publisher: ASME, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 2 vol. xxi+2223 pp.
ISBN: 0 7918 1559 5 Material Identity Number: XX-1999-01000
Conference Title: Proceedings of InterPACK '97
Conference Sponsor: ASME

Conference Date: 15-19 June 1997 Conference Location: Kohala Coast, HI, USA
Language: English
Abstract: The paper aims at implementing a computer-aided-engineering (CAE) approach for the complete thermal design and analysis of compact electronic enclosures. A laptop computer case study is introduced throughout this work. Modeling methodologies are discussed to simulate heat transfer in printed circuit boards and semiconductor packaging types encountered in portable electronics enclosures. Examples in the paper are based on a commercially available CFD-based thermal analysis tool, FLOTHERM, and cover integrated levels of compact enclosure packaging including system-, PCB- and semiconductor package-levels. System-level modeling of laptop enclosures are discussed including major entities and thermal enhancement options such as heat pipes. The paper introduces a simplified modeling approach to model the different signal/power traces in **FR4** -made PCBs. The results of the simplified model are compared to the detailed PCB model. A compact modeling methodology is introduced for the thermal modeling of a Tape Carrier Package (TCP) encountered in portable electronics enclosures. The compact model of the TCP package is integrated in a system-level model of a laptop enclosure and compared to a detailed model detailing the various entities inside the package.
Subfile: B C

11/3,AB/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC

6214916 INSPEC Abstract Number: B1999-05-2210-006
Title: Investigation of the correlation of peel strength and pad adhesion measurements using different printed **circuit board** base materials
Author(s): Mueller, S.
Author Affiliation: Hewlett-Packard GmbH, Boblingen, Germany
Conference Title: Twenty Third IEEE/CPMT International Electronics Manufacturing Technology Symposium (Cat. No.98CH36205) p.58-65
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xiv+491 pp.
ISBN: 0 7803 4523 1 Material Identity Number: XX-1998-03091
U.S. Copyright Clearance Center Code: 0 7803 4523 1/98/$10.00
Conference Title: Twenty Third IEEE/CPMT International Electronics Manufacturing Technology Symposium. Proceedings 1998 IEMT Symposium
Conference Sponsor: Semicond. Equipment & Mater. Int.; Componemts, Packaging & Manuf. Technol. Soc. IEEE
Conference Date: 19-21 Oct. 1998 Conference Location: Austin, TX, USA
Language: English
Abstract: The adhesion of pads to the PCB base material has, along with the assembly method, an essential impact on the reparability of components without damaging the PCB. Various test methods have been developed to evaluate Cu adhesion to different base materials. Two of those methods, the pad adhesion test and the peel strength test, have been investigated with the objective of finding the degree of correlation between the results obtained. A correlation of both methods would allow the use of the simpler measurement to obtain data about the more interesting parameter. In the test plan, the main factors influencing peel strength and pad adhesion are discussed, and the test matrix for both the initial and the main test is shown. The pad adhesion and peel strength measurement methods are explained, along with design of the test boards. The influence of the period between sample preparation (conventional print and etch process) and measurement, stripe width and stripe orientation at the base material on

the peel strength values and the effect of pad shape, number, size and pattern on the pad adhesion data is shown and discussed. After fixing the test parameters, the main measurements were made using a conventional **FR4** material. A correlation of pad adhesion and peel strength values has not been found due to the different fracture interfaces resulting from the different kinds of stress. A second test using Speedboard N/sup TM/ material showed a correlation of peel strength and pad adhesion data, based on the same fracture mode despite different kinds of stress.
Subfile: B

11/3,AB/21 (Item 21 from file: 2)
DIALOG(R)File 2:INSPEC

6157385 INSPEC Abstract Number: B1999-03-1350F-032
Title: A microwave analog frequency divider
Author(s): Vidmar, M.
Journal: Microwave Journal, Euro-Global Edition vol.41, no.11 p. 120, 122, 124, 126
Publisher: Horizon House Publications,
Publication Date: Nov. 1998 Country of Publication: USA
CODEN: MJEEET ISSN: 0192-6217
SICI: 0192-6217(199811)41:11L.120:MAFD;1-K
Material Identity Number: F336-1998-011
U.S. Copyright Clearance Center Code: 0192-6217/98/$5.00+1.00
Language: English
Abstract: A narrowband two-stage analog divide-by-four frequency divider that converts a 10 GHz input to 2.5 GHz. The circuit was constructed using HEMT devices on an **FR4** printed **circuit board** . The resulting circuit was used to provide the trigger input to a 10 GHz sampling oscilloscope and supplanted the need for obtaining a commercial flip-flop divider.
Subfile: B

11/3,AB/22 (Item 22 from file: 2)
DIALOG(R)File 2:INSPEC

6156472 INSPEC Abstract Number: B1999-03-1230B-005
Title: Wideband and low-noise microwave VCO
Author(s): Vidmar, M.
Journal: VHF Communications vol.30, no.4 p.210-25
Publisher: KM Publications,
Publication Date: Winter 1998 Country of Publication: UK
CODEN: VHFCEB ISSN: 0177-7505
SICI: 0177-7505(199824)30:4L.210:WNM;1-S
Material Identity Number: C311-1999-001
Language: English
Abstract: An important piece of radiofrequency or microwave test equipment is certainly the RF spectrum analyser. A spectrum analyser can be built by a skilled radio amateur. While most circuits of professional spectrum analysers can be reproduced in amateur conditions, the major problem is building a wideband, low-noise VCO for the first (swept) conversion. A varactor-tuned VCO covering the frequency band 2-4 GHz is presented. Such a VCO allows the design of a spectrum analyser with the first IF in the 2 GHz range, similar to professional instruments. The phase noise of the described VCO is reasonably low, within 20 dB of a

free-running YIG oscillator. Finally, the VCO design is fully reproducible using standard SMD parts mounted on a conventional **FR4** (0.8mm-thick) printed-**circuit board**.
Subfile: B

11/3,AB/23 (Item 23 from file: 2)
DIALOG(R)File 2:INSPEC

6127771 INSPEC Abstract Number: B1999-02-1130B-041, C1999-02-7410D-143
Title: Evaluating thermal characterization accuracy using CFD codes-a package level benchmark study of IcePak/sup TM/ and Flotherm/sup R/
Author(s): Zahn, B.A.
Author Affiliation: Package Characterization Lab., Abpac Inc., Phoenix, AZ, USA
Conference Title: ITherm'98. Sixth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (Cat. No.98CH36208) p. 322-9
Editor(s): Bhavnani, S.H.; Kormann, G.B.; Nelson, D.J.
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xv+541 pp.
ISBN: 0 7803 4475 8 Material Identity Number: XX-1998-01875
U.S. Copyright Clearance Center Code: 0 7803 4475 8/98/$10.00
Conference Title: ITherm'98. Sixth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems
Conference Sponsor: Components, Packaging, & Manuf. Technol. IEEE (CPMT/IEEE); Heat Transfer in Electron. Equipment Committee (K-16) of the Heat Transfer Div. ASME; NIST; Int. Microelectron. & Packaging Soc. (IMAPS)
Conference Date: 27-30 May 1998 Conference Location: Seattle, WA, USA
Language: English
Abstract: A benchmark thermal study was conducted using the IcePak/sup TM/ (ver. 2.01) and Flotherm/sup R/ (ver. 1.4) computational fluid dynamics (CFD) software packages. Both CFD applications were used to simulate the thermal performance of a 20-lead heatsink small outline package (20HSOP) in steady state natural convection environment. Five 20HSOP devices were tested while mounted on a Semiconductor Equipment and Materials (SEMI) standard **FR4** printed **circuit board** absent of any thermal enhancements and containing the minimum amount of copper traces needed for electrical connections. Power dissipations were varied to span a regime of radiation and natural convection heat transfer environments. Due to the symmetric nature of the problem, only half of the package/PCB was modeled. Each of the models utilized identical material thermal characteristics, dimensions, and boundary conditions. Simulation results were validated using experimental data at each device power dissipation. The simulated results obtained from both CFD tools agreed well with measured data (within 10%). However, in the majority of the experiments, IcePak computed junction and case temperatures which were slightly more accurate than those calculated by the Flotherm software, while also maintaining decreased run times. Model details are discussed along with the perceived advantages and disadvantages of the two CFD software packages.
Subfile: B C

11/3,AB/24 (Item 24 from file: 2)
DIALOG(R)File 2:INSPEC

6004724 INSPEC Abstract Number: B9810-0170J-013, C9810-7410D-026

01/06/2003

Title: Using design of experiment simulation responses to predict thermal performance limits of the heatsink small outline package (HSOP) considering both die bond and heatsink solder voiding
Author(s): Zahn, B.A.
Author Affiliation: Package characterization Lab., Abpac Inc., Phoenix, AZ, USA
Conference Title: Fourteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.98CH36195) p.153-60
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xvii+255 pp.
ISBN: 0 7803 4486 3 Material Identity Number: XX98-00768
U.S. Copyright Clearance Center Code: 0 7803 4486 3/98/$10.00
Conference Title: Fourteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium Proceedings 1998
Conference Sponsor: IEEE Components, Packaging, & Manuf. Technol. Soc
Conference Date: 10-12 March 1998 Conference Location: San Diego, CA, USA
Language: English
Abstract: This study provides a method to predict the steady state natural convection thermal performance limits of a heatsink small outline package (HSOP) when mounted on either an aluminum/polyimide or **FR4** printed **circuit board** . Analysis variables include the die area, power dissipation, die bond voiding, and package heatsink solder voiding. A 20-lead HSOP (20HSOP) was chosen for demonstration purposes. The methodology discussed herein can be easily applied to evaluate the thermal performance limits of other microelectronic packages. The method chosen to perform the analysis was a central composite design of experiments (CCD). An experimentally validated finite element analysis (FEA) model was used to predict theta /sub ja/ and psi /sub jc/ values for a series of twenty-five CCD simulations which encompassed the favored design space of the 20HSOP. The FEA model utilized a temperature dependent heat transfer coefficient which accounted for both natural convection and radiation heat transfer. The end product is a set of polynomial equations which allow the user to quickly predict the thermal capability of the package under various configurations.
Subfile: B C

11/3,AB/25 (Item 25 from file: 2)
DIALOG(R)File 2:INSPEC

5965597 INSPEC Abstract Number: B9808-0170J-093
Title: The strategy and status of a bare chip packaging
Author(s): Tsukada, Y.
Author Affiliation: Technol. Appl. Lab., IBM Japan Ltd., Yasu-gun, Japan
Conference Title: 1st 1997 IEMT/IMC Symposium (IEEE Cat. No.97CH36059) p.5-9
Publisher: SHM: Microelectron. Soc, Tokyo, Japan
Publication Date: 1997 Country of Publication: Japan xvi+415 pp.
ISBN: 0 7803 4235 6 Material Identity Number: XX98-00122
Conference Title: Proceedings of 1997 First International Electronic Manufacturing Technology (IEMT) IMC Symposium
Conference Sponsor: IEEE CPMT (Components, Packaging, & Manuf. Technol.) Soc.; SHM: Microelectron. Soc.-Japan
Conference Date: 16-18 April 1997 Conference Location: Tokyo, Japan
Language: English
Abstract: The first practical usage of bare chip packaging was achieved on a buildup printed **circuit board** with epoxy base material and a chip attachment to it by flip chip bonding. It was "Surface Laminar

Circuit and Flip Chip Attach (SLC/FCA)" from IBM Japan. The carrier technology, SLC, development was planned in 1986 as a future replacement of **FR4** printed **circuit board** . It was defined as a direct chip attach carrier in 1988 with a couple of others, Silicon on silicon and Copper polyimide carriers. Today, SLC is only one in production because of the performance and cost.
Subfile: B

11/3,AB/26 (Item 26 from file: 2)
DIALOG(R)File 2:INSPEC

5899833 INSPEC Abstract Number: B9806-1350F-009
Title: **FR4** PCB modulation transfer MW VCO up to 16 GHz
Author(s): Buoli, C.; Mora, G.; Cervi, L.A.
Author Affiliation: ITALTEL, Milan, Italy
Conference Title: 27th European Microwave 97 Conference and Exhibition. Bridging the Gap Between Industry and Academia. Conference Proceedings (IEEE Cat. No.97TH8317) Part vol.2 p.1058-63 vol.2
Publisher: ORTRA, Tel Aviv, Israel
Publication Date: 1997 Country of Publication: Israel 2 vol. 1366 pp.
Material Identity Number: XX97-02572
Conference Title: Proceedings of 27th Microwave Conference
Conference Date: 8-12 Sept. 1997 Conference Location: Jerusalem, Israel
Language: English
Abstract: The CPM modulation scheme allows microwave VCO phase locking to the IF signal: in this way the VCO output, provides directly the modulated RF carrier. The aim of this paper is to suggest the use of **FR4** as a microwave substrate to be able to reduce significantly the cost of the the VCO. thought, become determinant. By using the multilayer printed **circuit board**, the microwave structures (microstrip, stripline, matching networks) and the low frequency circuits (voltage regulator, alarms, loop filter) can be achieved working on the same substrate, resulting in a very low cost structure up to 16 GHz. Moreover, it is important to stress that it is possible to exploit SMT technology.
Subfile: B

11/3,AB/27 (Item 27 from file: 2)
DIALOG(R)File 2:INSPEC

5786262 INSPEC Abstract Number: B9802-2210D-015
Title: Alternatives to standard **FR4** materials
Author(s): Weiss, D.G.
Author Affiliation: Dielektra GmbH, Cologne, Germany
Conference Title: Recent Progress in Printed Circuit Board Technology p.6 pp.
Publisher: Fraunhofer-Inst. IZM, Berlin, Germany
Publication Date: 1997 Country of Publication: Germany 176 pp.
Material Identity Number: XX97-00847
Conference Title: Proceedings of 1997 Recent Progress in Printed Circuit Board Technology
Conference Date: 27-29 Jan. 1997 Conference Location: Berlin, Germany
Language: English
Abstract: Interconnection technology is increasing both circuit density and component density. In addition, new or modified assembly processes

demand better performance from the **circuit board** material. In certain applications, standard **FR4** is reaching its limits. For economic reasons, high performance resin systems are no longer a solution for the board designers. This paper explains how epoxy resin systems can be developed to build the bridge between the economic and technological requirements of the end users of printed circuit boards.
Subfile: B

11/3,AB/28 (Item 28 from file: 2)
DIALOG(R)File 2:INSPEC

5704147 INSPEC Abstract Number: B9711-2210D-005
Title: Thermal effects on PCB's with connectors during solder attachment
Author(s): Schluter, B.; De La Rosa, J.; Mattsen, R.; Pearsall, K.
Author Affiliation: IBM Corp., Austin, TX, USA
Conference Title: 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048) p.1120-3
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 1294 pp.
ISBN: 0 7803 3857 X Material Identity Number: XX97-01595
U.S. Copyright Clearance Center Code: 0 7803 3857 X/97/$4.00
Conference Title: 1997 Proceedings 47th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Conference Date: 18-21 May 1997 Conference Location: San Jose, CA, USA
Language: English
Abstract: With the increasing complexity of electronic assemblies, a greater number of interconnections between electronic cards are needed. In many cases, longer and higher density connectors are being used to supply this increased number of interconnections. As such the match of the thermal expansion of the printed **circuit board** (PCB) to that of the connectors is becoming more critical for proper assembly. This paper explores the dimensional changes to the card assemblies as these pin-in-hole (PIH) connectors and other large components are soldered to the card during the wave solder process. The relevant characteristics of both the connectors and the **FR4** material are evaluated and the contributions of the significant processing variables are discussed. This includes the dimensional changes to the PCB and the connectors around the glass transition temperature and the melting temperature of the eutectic solder used in the wave solder machine. The distortion due to asymmetrical board lay-up is discussed independently. These effects are then related to the overall flatness of the card assembly after completion of the process. In conclusion there are some recommendations to minimize these effects for specific applications.
Subfile: B

11/3,AB/29 (Item 29 from file: 2)
DIALOG(R)File 2:INSPEC

5665014 INSPEC Abstract Number: B9709-0560-020
Title: Primerless RTV silicones for electronic protection
Author(s): Van Wert, B.; Fiori, J.
Author Affiliation: Dow Corning Corp., Midland, MI, USA
Conference Title: Proceedings. 3rd International Symposium on Advanced

01/06/2003

Packaging Materials Processes, Properties and Interfaces (Cat. No.97TH8263) p.54-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA viii+183 pp.
ISBN: 0 7803 3818 9 Material Identity Number: XX97-00693
Conference Title: Proceedings 3rd International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces
Conference Sponsor: Int. Microelectron. & Packaging Soc. (IMAPS); IEEE Components, Packaging, & Manuf. Technol. Soc.; Georgia Inst. Technol., Pakcaging Res. Center (PRC)
Conference Date: 9-12 March 1997 Conference Location: Braselton, GA, USA
Language: English
Abstract: This paper describes a new silicone potting compound, which has been formulated to deliver fast, room-temperature vulcanizing (RTV) cure and excellent adhesion to most common metals and plastics in electronics applications. Dow Corning(R) 3-4207 Gel has been tested with good results on aluminum, alumina, and copper, as well as PET, **FR4** board, and PPS. The material has demonstrated excellent performance on the high-temperature epoxy glass laminates used in **circuit board** manufacturing. With difficult substrates, a 15-30 minute cure cycle at 60-80 degrees C has been shown to produce excellent interfacial adhesion.
Subfile: B

11/3,AB/30 (Item 30 from file: 2)
DIALOG(R)File 2:INSPEC

5584371 INSPEC Abstract Number: B9706-0170J-076
Title: Evaluation of isothermal and isoflux natural convection coefficient correlations for utilization in electronic package level thermal analysis
Author(s): Zahn, B.A.; Stout, R.P.
Author Affiliation: Motorola Inc., Tempe, AZ, USA
Conference Title: Thirteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.97CH36031) p.24-31
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA xvi+291 pp.
ISBN: 0 7803 3793 X Material Identity Number: XX97-00364
U.S. Copyright Clearance Center Code: 0 7803 3793 X/97/$5.00
Conference Title: Thirteenth Annual IEEE. Semiconductor Thermal Measurement and Management Symposium
Conference Sponsor: IEEE Components, Packaging, & Manuf. Technol. Soc
Conference Date: 28-30 Jan. 1997 Conference Location: Austin, TX, USA
Language: English
Abstract: A 20-lead heatsink small outline package (20HSOP) was modeled on both an **FR4** and aluminum printed **circuit board** using a solid model finite element simulation tool. Three different correlations (isothermal, single surface isoflux, and dual surface isoflux) were utilized to define the surface convection coefficients of both the package and printed **circuit board** in a natural convection cooled environment. Solid model temperature results were compared to physical measurements in order to evaluate the usefulness of the individual convection coefficient correlations for package level thermal analysis. Both the experimental and solid model simulation results were also compared to those obtained from an identical computational fluid dynamics (CFD) model of the 20HSOP package. The isothermal convection coefficient correlations provided the most accurate solid model simulation results (within 12%) when using the **FR4** thermal characterization test board. The isoflux dual surface convection coefficient correlations provided the

most accurate solid model simulation results (within 13%) when using the aluminum thermal characterization test board. Solid model solutions closely matched, and in some cases exceeded, the accuracy of the CFD model. The significance of these results to package level thermal analysis is discussed.
Subfile: B

11/3,AB/31 (Item 31 from file: 2)
DIALOG(R)File 2:INSPEC

5566565 INSPEC Abstract Number: B9706-2210B-004
Title: A low cost, multi-layer **FR4 circuit board** for the rf and microwave circuits in a fixed wireless access residential transceiver unit
Author(s): Broome, K.R.
Author Affiliation: Nortel Ltd., Paignton, UK
Conference Title: IEE Colloquium on RF and Microwave Circuits for Commercial Wireless Applications (Ref. No.1997/026) p.5/1-6
Publisher: IEE, London, UK
Publication Date: 1996 Country of Publication: UK 78 pp.
Material Identity Number: XX97-00748
Conference Title: IEE Colloquium on RF & Microwave Circuits for Commercial Wireless Applications
Conference Sponsor: IEE
Conference Date: 13 Feb. 1997 Conference Location: London, UK
Language: English
Abstract: The choice of printed **circuit board** is an important factor in the design of rf and microwave circuits: it influences many issues such as overall product cost, ease of manufacture, circuit electrical performance and reliability. A multi-layer, epoxy/glass multi-functional **FR4** board has been used for the rf and microwave circuitry in Nortel's "Proximity I" Residential Transceiver Unit. This unit forms part of the Residential Subscriber System of the Ionica Fixed Wireless Access telephone system. This paper describes various important features of the Residential Transceiver Unit **circuit board** relevant to its manufacture in high volume. Theoretical and experimental data is presented both for the performance of the board itself and also of some of the rf and microwave circuitry mounted on it.
Subfile: B

11/3,AB/32 (Item 32 from file: 2)
DIALOG(R)File 2:INSPEC

5546140 INSPEC Abstract Number: B9705-0100-073
Title: IEE Colloquium on RF & Microwave Circuits for Commercial Wireless Applications
Publisher: IEE, London, UK
Publication Date: 1996 Country of Publication: UK 78 pp.
Material Identity Number: XX97-00748
Conference Title: IEE Colloquium on RF & Microwave Circuits for Commercial Wireless Applications
Conference Sponsor: IEE
Conference Date: 13 Feb. 1997 Conference Location: London, UK
Language: English
Abstract: The following topics are covered: RF ICs for GPS applications;

ceramic RF circuits for high volume wireless products; RF front-end for V-SCADA communication networks; 1.6 watt, 1.9 GHz power amplifier MMIC in silicon; low cost, multi-layer, **FR4 circuit board** for the RF and microwave circuits in a fixed wireless access residential transceiver unit; low cost design techniques for RF circuits in consumer electronics; front end building blocks using the Glasgow 0.2 mu m GaAs MESFET process; and GaAs MMICs for 5.2 GHz HIPERLAN.
Subfile: B

11/3,AB/33 (Item 33 from file: 2)
DIALOG(R)File 2:INSPEC

5442849 INSPEC Abstract Number: B9701-2210D-045
Title: New laser processes and wavelengths for drilling through-hole and blind vias in a wide range of **circuit board** materials
Author(s): Cable, A.
Author Affiliation: Electro Sci. Ind. Inc., Portland, OR, USA
Conference Title: Proceedings of the Technical Conference IPC Printed Circuits EXPO '96 p.S18/5/1-9
Publisher: IPC, Northbrook, IL, USA
Publication Date: 1996 Country of Publication: USA 762 pp.
Material Identity Number: XX96-00763
Conference Title: Proceedings of Printed Circuits Conference
Conference Date: 3-7 March 1996 Conference Location: San Jose, CA, USA
Language: English
Abstract: Earlier work using a solid-state ultraviolet laser operating at 266 nm, with peak powers in excess of 5 kW, has shown UV lasers to be very capable tools for micro-via formation in a wide range of **circuit board** materials. These materials include glass reinforced **FR4**, aramid reinforced epoxies, nonreinforced epoxy and PTFE compositions. The recent development by Electro Scientific Industries Inc. of a more powerful solid-state ultraviolet laser operating at 355 nm with peak powers in excess of 12 kW has allowed this work to be extended. Drilling experiments have shown very similar via quality to the 266 nm laser. Significant throughput improvements in some drilling processes have been recorded.
Subfile: B

11/3,AB/34 (Item 34 from file: 2)
DIALOG(R)File 2:INSPEC

5418178 INSPEC Abstract Number: B9612-2210B-009
Title: Printed **circuit board** material and design considerations for wireless applications
Author(s): Daigle, B.
Author Affiliation: Lurie R&D Centre, Rogers Corp., Rogers, CT, USA
Conference Title: 1996 Proceedings. 46th Electronic Components and Technology Conference (Cat. No.96CH35931) p.354-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA 1311 pp.
ISBN: 0 7803 3286 5 Material Identity Number: XX96-01869
U.S. Copyright Clearance Center Code: 0 7803 3286 5/96/$4.00
Conference Title: 1996 Proceedings 46th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc

Conference Date: 28-31 May 1996 Conference Location: Orlando, FL, USA
Language: English
Abstract: Designers are moving towards material systems which can be fabricated using conventional epoxy/glass printed **circuit board** (PCB) processes. This allows microwave circuits to be built using the vast fabrication infrastructure available for digital circuits. This paper provides basic background information about substrate material characteristics and design considerations, which are critical for wireless applications. Material characteristics discussed include dissipation factor, dielectric constant tolerances and stability. Design and material options which allow microwave circuits to be manufactured by conventional **FR4** fabricators are emphasized.
Subfile: B

11/3,AB/35 (Item 35 from file: 2)
DIALOG(R)File 2:INSPEC

5183309 INSPEC Abstract Number: B9603-2210D-065
Title: Additive printed **circuit board** process using Ormet ink
Author(s): Roberts, E.D.
Author Affiliation: North Iowa Electron., IA, USA
Conference Title: Proceedings of the Technical Program. NEPCON WEST `95 Part vol.3 p.1249-53 vol.3
Publisher: Reed Exhibition Companies, Norwalk, CT, USA
Publication Date: 1995 Country of Publication: USA 3 vol. 1994 pp.
Material Identity Number: XX95-03009
Conference Title: Proceedings NEPCON West 95
Conference Date: 26 Feb.-2 March 1995 Conference Location: Anaheim, CA, USA
Language: English
Abstract: The making of printed circuit boards (PCBs) using an additive process, as opposed to using the conventional subtractive process, can now be performed with high duality and repeatability. The additive ink, called Ormet, is a metallic based ink which is a combination of metal powders and polymers that, when fused, form a continuous metallic structure that bonds to a substrate material. In a typical application, the ink is applied to the substrate material, e.g. **FR4**, using a screen printer and when properly cured, forms an additive process circuit that has high conductivity, adhesion and solderability.
Subfile: B

11/3,AB/36 (Item 36 from file: 2)
DIALOG(R)File 2:INSPEC

4922896 INSPEC Abstract Number: B9505-2210D-028
Title: Moisture absorption behavior of printed circuit laminate materials
Author(s): Liu, P.C.; Wang, D.W.; Livingston, E.D.; Chen, W.T.
Author Affiliation: Electron. Packaging, IBM Corp., Endicott, NY, USA
Part vol.1 p.435-42 vol.1
Editor(s): Engel, P.A.; Chen, W.T.
Publisher: ASME, New York, NY, USA
Publication Date: 1993 Country of Publication: USA 2 vol. xi+1200 pp.
ISBN: 0 7918 0686 3
Conference Title: Proceedings of Electronic Packaging Conference
Conference Sponsor: ASME

Conference Date: 29 Sept.-2 Oct. 1993 Conference Location: Binghamton, NY, USA

Language: English

Abstract: The reliability of a printed **circuit board** is strongly influenced by the presence of moisture. High levels of moisture can cause internal shorts through metal migration, delamination during soldering processes, poor electronic and mechanical performance, and varying dimensional stability. With the broader utilization of printed circuit technology in electronics products, such as wireless personal communication systems, resin systems with more robust moisture capabilities would be very important, especially in applications such as multi-chip modules on laminates (MCM-L) and chips-on-board (COB). Thus, it is necessary to understand the moisture absorption behavior of printed circuit laminates. The moisture absorption characteristics of **FR4**, Driclad, and bismaleimid-triazine (BT) resins and their laminates were investigated gravimetrically in this study. Driclad epoxy, a new resin with a high glass transition temperature, has been qualified and introduced to the market at IBM Endicott. Experiments including the vapor exposure to 80%, relative humidity at 35, 50, and 85 degrees C and liquid immersion at 23 and 100 degrees C were performed. In addition, the dimensional change of neat resins and the glass transition temperature of resins and resin-glass laminates were measured as a function of moisture content. Diffusion coefficient, the activation energy of diffusion and maximum moisture weight gain were determined. At the initial absorption stage. Fickian diffusion behavior was observed for all samples. The maximum moisture weight gain and diffusion coefficient in descending order were found to be **FR4**, BT, Driclad, and BT, Driclad, **FR4** respectively. **FR4** resin picked up about twice much moisture as Driclad resin. The maximum moisture weight gain of **FR4** increases with increasing temperature, while Driclad and BT depend only slightly on temperature. The T/sub g/ decreases with increasing moisture content. The Driclad laminate is more robust to the soldering process than the **FR4** laminate. From the moisture weight gain, diffusion coefficient, and solder shock data, Driclad is considered to have the best moisture resistance among the resins used in this study.

Subfile: B

11/3,AB/37 (Item 37 from file: 2)
DIALOG(R)File 2:INSPEC

04064949 INSPEC Abstract Number: B9202-2210D-080, C9202-7410H-160

Title: Reliability Monitoring in drilling electronic circuit boards

Author(s): Hocheng, H.; Jiaa, C.L.

Author Affiliation: Dept. of Power Mech. Eng., Nat. Tsing Hua Univ., Hsinchu, Taiwan

Journal: Transactions of the ASME. Journal of Electronic Packaging vol.113, no.3 p.263-7

Publication Date: Sept. 1991 Country of Publication: USA

CODEN: JEPAE4 ISSN: 1043-7398

Language: English

Abstract: The purpose of the current study is to provide a monitoring scheme for evaluating the reliability of drilling of electronic **circuit board** (ECB) made of **FR4** composite materials. The ECB is a laminated mechanical structure. Delamination often occurs at the hole exit during drilling. The resulted delamination deteriorates the long-term performance of the ECB when subject to mechanical and/or thermal loading. Acoustic emission can monitor the extent of this damage. A linear relationship exists between the size of delamination and the energy level of emitted signal when the proposed signal processing technique is used.

The results contribute to higher quality ECB's and can be applied in the manufacturing stage in an automated manner.
Subfile: B C

11/3,AB/38 (Item 38 from file: 2)
DIALOG(R)File 2:INSPEC

03848395 INSPEC Abstract Number: B91022887, C91025044
Title: Substrate impact on the thermal performance of tape automated bonding components
Author(s): Davis, T.L.
Author Affiliation: IBM Corp., Austin, TX, USA
Journal: IEEE Transactions on Components, Hybrids, and Manufacturing Technology vol.13, no.4 p.998-1005
Publication Date: Dec. 1990 Country of Publication: USA
CODEN: ITTEDR ISSN: 0148-6411
U.S. Copyright Clearance Center Code: 0148-6411/90/1200-0998$01.00
Language: English
Abstract: The results of thermally characterizing a 160-I/O (input/output) tape automated bonding (TAB) device are reported. A finite-element technique is used to understand and model the thermal processes of the TAB. A three-dimensional (3-D) computer model is developed and validated against experimental data obtained in a natural convection environment. The 3-D model's results indicate that the thermal processes associated with the TAB are not 2-D in nature. A substantial temperature variation is present across much of the device. Several carriers are modeled with the TAB device to determine their thermal effect on the device's thermal characteristics. Reducing the card's cross-section from a multilayer printed **circuit board** (PCB) to a board with no internal planes substantially impacts the power dissipation capabilities of the component. The use of a molded rather than an **FR4** material in the card has a negligible effect on the thermal characteristics of the attached device due to their similar thermal conductivity.
Subfile: B C

11/3,AB/39 (Item 39 from file: 2)
DIALOG(R)File 2:INSPEC

03809926 INSPEC Abstract Number: B91007604, C91012627
Title: Thermal characteristics of surface mount packages
Author(s): Kelly, E.G.
Author Affiliation: Philips Components, Smithfield, RI, USA
Conference Title: Competitive Surface Mount Technology. The Proceedings of SMTCON. Surface Mount Technology Conference and Exposition p.127-37
Publisher: IC Manage, Chicago, IL, USA
Publication Date: 1990 Country of Publication: USA 476 pp.
Conference Date: 3-6 April 1990 Conference Location: Atlantic City, NJ, USA
Language: English
Abstract: This report describes the modeling of two well-known surface mount outlines: the SOT-23 and SOT-89 and the new SOT-223 using computer simulations under realistic application conditions (both **FR4** printed **circuit board** and ceramic substrate mounting were modeled). In addition, the effect of extraneous conditions (of mounting, soldering etc.) were examined in detail. Finally, the theoretical results were compared with actual measurements and the differences explained. This represents the most comprehensive analysis to date on the thermal characteristics of these

surface mount components.
Subfile: B C

11/3,AB/40 (Item 40 from file: 2)
DIALOG(R)File 2:INSPEC

03735370 INSPEC Abstract Number: B90070683, C90066196
Title: A closed form analytical model for the electrical properties of microstrip interconnects
Author(s): Bogatin, E.
Author Affiliation: Xinix Inc., Santa Clara, CA, USA
Journal: IEEE Transactions on Components, Hybrids, and Manufacturing Technology vol.13, no.2 p.258-66
Publication Date: June 1990 Country of Publication: USA
CODEN: ITTEDR ISSN: 0148-6411
U.S. Copyright Clearance Center Code: 0148-6411/90/0600-0258$01.00
Language: English
Abstract: A simple model is presented based on closed-form analytical approximations for the resistance, capacitance, inductance, and conductance of a generic microstrip interconnect. Working in the frequency domain, all the low-frequency lumped circuit and high-frequency transmission line properties can be calculated. As examples, this model is applied to high-frequency reflectivity measurements on Teflon and **FR4** printed **circuit board** microstrips. Agreement to better than 5% up to 1 GHz is obtained by using a dielectric constant of 2.20 and dissipation factor of 0.004 for the Teflon boards and a dielectric constant of 4.9 at 1 MHz with a constant dissipation factor of 0.022 for the **FR4** microstrips. This model enables packaging engineers to evaluate the possibilities of an interconnect technology very simply on their personal computers (PCs).
Subfile: B C

11/3,AB/41 (Item 41 from file: 2)
DIALOG(R)File 2:INSPEC

03720004 INSPEC Abstract Number: B90060977
Title: Solder joint reliability of fine pitch solder bumped pad array carriers
Author(s): Moore, K.; Machuga, S.; Bosserman, S.; Stafford, J.
Author Affiliation: Motorola Inc., Schaumburg, IL, USA
Conference Title: Proceedings of the Technical Program of the National Electronic Packaging and Production Conference. NEPCON West '90 p.264-74 vol.1
Publisher: Cahners Exposition Group, Des Plaines, IL, USA
Publication Date: 1990 Country of Publication: USA 2 vol. 1856 pp.
Conference Date: 26 Feb.-1 March 1990 Conference Location: Anaheim, CA, USA
Language: English
Abstract: It is well known that solder joint fatigue during thermal cycling is a problem when large surface mount leadless ceramic chip carriers are soldered to conventional **FR4** printed circuit boards. Solutions to this problem have been developed. With proper board level interconnect design, an 0.85 in square solder bumped ceramic pad array carriers (PAC) was reliably attached to a printed **circuit board**. Solder joint reliability was experimentally verified by temperature cycling and in situ continuous resistivity monitoring of the solder joint. Results on standard **FR4** PCB show that the solder alloy and the solder

joint geometry can make a factor of 10 difference in the temperature cycle life of the solder joint. Also, on an **FR4** PCB, it was determined that an epoxy underfill improves the thermal cycle life of the PAC solder joint by factor of 5. It was shown that a PAC soldered to a novel low CTE aramid paper/epoxy PCB can withstand 1000 temperature cycles without a failure. A brief discussion of the origin of the improved reliability of the various configurations of the large surface mount ceramic pad array chip carriers is given.
Subfile: B

11/3,AB/42 (Item 42 from file: 2)
DIALOG(R)File 2:INSPEC

2239385 INSPEC Abstract Number: B84024613
Title: Surface mounted IC packages-their attachment and reliability on PWBs
Author(s): Brierley, C.J.; Pedder, D.J.
Author Affiliation: Plessey Res. (Caswell) Ltd., Towcester, UK
Journal: Circuit World vol.10, no.2 p.28-31
Publication Date: 1984 Country of Publication: UK
CODEN: CIWODV ISSN: 0305-6120
Material Identity Number: C183-84001
Language: English
Abstract: This paper discusses the evaluation of two soldering techniques for the attachment of the chip carrier and SOIC packages to epoxy glass PWBs: the first by solder cream printing or pretinning of the **circuit board** and subsequent attachment by solder reflow, and the second by a novel jet soldering technique. The thermally induced expansion mismatch between epoxy glass and ceramic chip carriers and the strain induced fatigue this causes in the solder joints are now well documented, and results are presented for the effects of temperature cycling ceramic chip carriers soldered onto PWBs. Various PWB materials have been assessed including **FR4** elastomer coated **FR4**, polyimide kevlar, and epoxy glass laminated copper clad invar. Reliability of these assemblies is discussed in terms of the appearance of micro-cracks in the solder fillets and the occurrence of electrical discontinuity in the solder joints during temperature cycling.
Subfile: B

11/3,AB/43 (Item 43 from file: 2)
DIALOG(R)File 2:INSPEC

02160851 INSPEC Abstract Number: B84000999
Title: Solderable and wire bondable conductive polymer circuitry
Author(s): Keitel, G.A.
Author Affiliation: Methode Dev. Co., Chicago, IL, USA
Conference Title: Northcon/82 Conference Record p.9/4/1-6
Publisher: Electron. Conventions, El Segundo, CA, USA
Publication Date: 1982 Country of Publication: USA 484 pp.
Conference Date: 18-20 May 1982 Conference Location: Seattle, WA, USA
Language: English
Abstract: Printed wire circuits produced with polymer conductive materials on low temperature boards which are fully wire bondable and solderable are now being made. Application of a plated metal surface over the printed thick film polymer conductor pattern makes this possible. The printed polymers currently being used for this type of board construction are thermal set epoxy silver conductors. Also available is a low cost,

non-noble nickel polymer. Ultraviolet curable silver applied on a **FR4** **circuit board** was also made solderable by an over plating of electroless nickel. The plating currently being applied is an electroless bath of either nickel boron or nickel phosphorus. The plating solutions are readily available from a number of commercial suppliers. Experimental samples can be easily produced using pyrex glassware and a laboratory hot plate.
Subfile: B

11/3,AB/44 (Item 44 from file: 2)
DIALOG(R)File 2:INSPEC

01409010 INSPEC Abstract Number: B79042211, C79026079
Title: Improved printed-**circuit board** dynamic characteristics using structural damping ribs
Author(s): Hain, H.L.; Patel, B.M.
Conference Title: Proceedings of the IEEE 1979 National Aerospace and Electronics Conference NAECON 1979 Part I p.222-32
Publisher: IEEE, New York, NY, USA
Publication Date: 1979 Country of Publication: USA 500 pp.
Conference Sponsor: IEEE
Conference Date: 15-17 May 1979 Conference Location: Dayton, OH, USA
Language: English
Abstract: Introduces a new concept for reducing the vibrations of printed-circuit boards due to external sources. The configurations and geometric locations of structural damping ribs on the printed-**circuit board** are described. The response characteristics of thin, simply supported-free-simply supported-free, (SS-F-SS-F) **FR4** epoxy composite printed-circuit boards are described in the frequency range of 15 to 2500 Hz. Test data representing the effectiveness of the damping ribs are presented. The addition of structural damping ribs is found to be effective in controlling vibrations of printed-circuit boards.
Subfile: B C

11/3,AB/45 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

0883494 NTIS Accession Number: N81-17113/4/XAB
Internal Electrostatic Discharge Hazard Risk Assessment to the Galileo Orbiter
(Final Report)
Schmidt, R. E. ; Andrews, J. C. ; Treadaway, M. J. ; Leadon, R. E.
General Electric Co., Philadelphia, PA. Space Div.
Corp. Source Codes: 009193019; GK087134
Sponsor: National Aeronautics and Space Administration, Washington, DC.
Report No.: NASA-CR-163930
27 Oct 80 40p
Languages: English
Journal Announcement: GRAI8113; STAR1908
Prepared for JPL.
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NTIS Prices: PC A03/MF A01
A worst case assessment was performed on the Command Data System (CDS) multilayer printed **circuit board** and an output power

transformer module in the power subsystem. An estimate of the Jovian environment during the 35 hour orbit insertion was supplied by JPL and used as an input to calculate the electron transport into the Galileo components. A radiation shielding analysis computer code, CHARGE, calculated the electron transport deposition trapped in the anticipated sensitive areas of the multilayer board and transformer module. Based on these trapped charge calculations electric fields were calculated between the identified isolated areas and the spacecraft ground. The results of the assessment of electrostatic discharge (DSD) in the CDS multilayer printed **circuit board** indicate that the probability of ESD in the **FR4** is low. The probability of ESD in the components attached to the multilayer board, however, is uncertain based on a lack of prior experimental data.

11/3,AB/46 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

11192874 Genuine Article#: 619LZ Number of References: 7
Title: Micro-assembled multi-chamber thermal cycler for low-cost reaction chip thermal multiplexing (ABSTRACT AVAILABLE)
Author(s): Zou QB; Miao YB (REPRINT) ; Chen Y; Sridhar U; Chong CS; Chai TC ; Tie Y; Teh CHL; Lim TM; Heng C
Corporate Source: Inst Microelect,Singapore//Singapore/ (REPRINT); Inst Microelect,Singapore//Singapore/; Natl Univ Singapore,Dept Biol Sci,Singapore 0511//Singapore/; Natl Univ Singapore,Dept Paediat,Singapore 0511//Singapore/
Journal: SENSORS AND ACTUATORS A-PHYSICAL, 2002, V102, N1-2 (DEC 1), P 114-121
ISSN: 0924-4247 Publication date: 20021201
Publisher: ELSEVIER SCIENCE SA, PO BOX 564, 1001 LAUSANNE, SWITZERLAND
Language: English Document Type: ARTICLE
Abstract: This paper presents a miniaturised multi-chamber thermal cycler capable of thermal multiplexing for high throughput polymerase chain reaction (PCR) of nucleic acids, using low-cost reaction chip. The thermal cycler has been fabricated in a micro-assembly manner using flip-chip bonding technique, which is batch manufacturable with good reproducibility. Silicon heating blocks in the multi-chamber array are mounted on a printed-**circuit-board** (PCB) substrate, with the later attached to a metal plate heat sink. Thermal cross-talk has been minimised by using thin and low thermal conductivity PCB. The preferred reaction chip containing multiple chambers is made of low-cost plastics, while other PCR compatible materials are also possible. The preliminary experiments show that with up to 20 mul sample in the thermally formed plastic chip, a full speed of 8 min for 30-cycle PCR is achievable. Thermal cross-talk of as less as 0.2% is obtained with the very thin PCB substrate (500 mum, **FR4**) and the plastic chip (100 mum PET), in a standard format of multi-chamber array. A temperature fluctuation of +/-0.1degreesC has been achieved during thermal multiplexing of up to 16 chambers, with each chamber consuming an average heating power of no more than 1.2 W. Finite element analysis (FEA) is conducted to optimise the thermal performance of the cycler. Experiments are in well agreements with the simulations.

11/3,AB/47 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01/06/2003

10851462 Genuine Article#: 573XW Number of References: 9
Title: Improving signal integrity in circuit boards by incorporating embedded edge terminations (ABSTRACT AVAILABLE)
Author(s): Adsure V (REPRINT) ; Kroger H; Shi WM
Corporate Source: Eastman Kodak Co,Rochester//NY/14650 (REPRINT); Eastman Kodak Co,Rochester//NY/14650; SUNY Binghamton,Watson Sch, Dept Elect Engn,Binghamton//NY/13902
Journal: IEEE TRANSACTIONS ON ADVANCED PACKAGING, 2002, V25, N1 (FEB), P 12-17
ISSN: 1521-3323 Publication date: 20020200
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA
Language: English Document Type: ARTICLE
Abstract: Much attention has been paid toward signal and power integrity in devices, circuit boards as well as entire systems. Resonances set up between the power and ground planes due to multiple reflections from the edges of the **circuit board** will affect signal integrity. The impedance seen by a via passing between the power and ground planes can be very high at the resonant frequencies. This gives rise to the effects of crosstalk and simultaneous switching noise (SSN) which would adversely effect the operation of the device. An attempt has been made in this paper to cover all the topics in [1] and [2], which describe a method to incorporate lossy (absorbing) material at the edges of a **circuit board** to reduce the wave reflections. The "lossy material" is usually a material of very high resistivity but which shows large magnetic losses at UHF and microwave frequencies [3]. Thus this material is suitable to be placed directly between the power and ground planes without introducing any dc leakage currents. Experiments were carried out on a bare copper **circuit board** with a **FR4** dielectric. The absorber used in the experiments is available commercially in flexible, castable and a hard dense form. It is shown that it is possible to reduce the impedances at the resonant frequencies to quite an extent over a broad frequency band by applying the lossy material at the edges of the board. Various configurations of applying the material are also described.

11/3,AB/48 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

09558863 Genuine Article#: 420BZ Number of References: 6
Title: An integrated micro cooling system for electronic circuits (ABSTRACT AVAILABLE)
Author(s): Schutze J (REPRINT) ; Ilgen H; Fahrner WR
Corporate Source: ILFA GmbH,D-01723 Kesselsdorf//Germany/ (REPRINT); ILFA GmbH,D-01723 Kesselsdorf//Germany/; Fern Univ Hagen,Dept Elect Devices,D-58084 Hagen//Germany/
Journal: IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, 2001, V48, N2 (APR) , P281-285
ISSN: 0278-0046 Publication date: 20010400
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA
Language: English Document Type: ARTICLE
Abstract: A fully **FR4**-compatible integrated cooling system has been developed. Cooling channels have been etched into a thick copper lay er to form microchannels. The structure is reinforced by two prepreg layers toward the component and solder side. Several cooling channels can be independently run. The heat dissipation capability of the system is 20 W per channel (and heat source). Typical coolants are water or methoxynonafluorobutane. For an outlet to inlet temperature difference

of 25 degreesC and a power dissipation of 30 W, a (water) flow rate of 20 mL/min is required. Pressure losses are below 300 mbar (for water).

11/3,AB/49 (Item 4 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08818777 Genuine Article#: 332HK Number of References: 0
Title: Lightweight **circuit board** material takes on **FR4**
Author(s): ANONYMOUS
Journal: ELECTRONICS WORLD, 2000, V106, N1772 (AUG), P598-598
ISSN: 0959-8332 Publication date: 20000800
Publisher: REED BUSINESS INFORMATION LTD, QUADRANT HOUSE THE QUADRANT, SUTTON SM2 5AS, SURREY, ENGLAND
Language: English Document Type: NEWS ITEM

11/3,AB/50 (Item 5 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06650393 Genuine Article#: ZH454 Number of References: 4
Title: Halogen-free flame-retardant plastics for electronic applications (ABSTRACT AVAILABLE)
Author(s): VonGentzkow W; Huber J; Kapitza H; Rogler W
Corporate Source: SIEMENS AG,CORP RES & DEV/D-8520 ERLANGEN//GERMANY/
Journal: JOURNAL OF VINYL & ADDITIVE TECHNOLOGY, 1997, V3, N2 (JUN), P 175-178
ISSN: 0193-7197 Publication date: 19970600
Publisher: SOC PLASTICS ENG INC, 14 FAIRFIELD DR, BROOKFIELD, CT 06804-0403
Language: English Document Type: ARTICLE
Abstract: In order to meet international standards, printed **circuit board** (PCB) base materials have to be flame-retardant according to the UL 94V specification. Up to now this has been achieved with **FR4** materials by using brominated aromatic components. **FR4** materials are glass epoxy based and are by far most prevalent in PCB production. Unfortunately, in the case of fire or smoldering, these materials evolve highly corrosive, and, under unfavorable conditions, even highly toxic decomposition products. In the search for flame retardancy without the use of bromine, the effect of different structural elements on the burning behavior of cured resins has been investigated. As a result of these investigations an epoxy resin was developed that contains tailor-made N- and P-containing constituents that form flame-retardant structures during processing and curing of the material. The new material meets all requirements for printed circuit boards and can be processed without any need to modify established technologies. Analytical and ecotoxicological investigations of the combustion products of the new material show that they are comparable with those of wood from the beech tree. PCBs and electronic assemblies manufactured therefrom successfully passed all functional tests. The base materials recently became commercially available.

11/3,AB/51 (Item 6 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

04915259 Genuine Article#: UR417 Number of References: 10
Title: LASER SOLDERING AND INSPECTION OF FINE-PITCH ELECTRONIC COMPONENTS

01/06/2003

(Abstract Available)
Author(s): FLANAGAN A; CONNEELY A; GLYNN TJ; LOWE G
Corporate Source: NATL UNIV IRELAND UNIV COLL GALWAY,NATL CTR LASER APPLICAT/GALWAY//IRELAND/
Journal: JOURNAL OF MATERIALS PROCESSING TECHNOLOGY, 1996, V56, N1-4 (JAN), P531-541
ISSN: 0924-0136
Language: ENGLISH Document Type: ARTICLE
Abstract: The increasing miniaturisation of integrated circuits has resulted in devices with lead spacings as small as 0.008 ''. Laser soldering has the potential to overcome many of the problems encountered with these devices by conventional soldering technologies. Nd:YAG laser soldering of a 224-lead ceramic chip onto a **FR4 circuit board** is described, using experimental design to optimise the laser parameters for soldering. In order to improve solder joint quality and repeatability, a rigorous thermal analysis is undertaken using a finite element model to investigate the temperature rise variations between the joints. Thermocouple measurements are made in real time of the laser soldering process to confirm the finite element model predictions.

11/3,AB/52 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01859200 AADAAI3034872
Experimental and numerical evaluation of embedded capacitance for power bus noise suppression in multi-layer printed **circuit board** designs
Author: Xu, Minjia
Degree: Ph.D.
Year: 2001
Corporate Source/Institution: University of Missouri - Rolla (0135)
Source: VOLUME 62/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 5296. 100 PAGES
ISBN: 0-493-47646-6

Embedded capacitance is a promising alternative to discrete decoupling capacitors for power bus noise mitigation. In this research work, experimental and numerical techniques are developed and applied to evaluate embedded capacitance in multi-layer printed **circuit board** designs. First, the electrical performance of embedded capacitance boards is measured and compared to standard **FR4** boards. Measurement results show that unlike discrete decoupling capacitors, embedded capacitance can efficiently reduce power bus noise over a broad frequency range.

To understand the power bus noise performance of embedded capacitance boards, the fundamental properties of closely-spaced power-retum plane pairs are further explored. A cavity model is applied to characterize the rectangular power-retum plane structures because this model is relatively simple yet reasonably intuitive. Using the cavity model, the effects of various loss mechanisms are examined for typical embedded capacitance boards. The important role of the conductive loss is revealed. The validity of the cavity model for lossy power-return plane structures is also investigated. Finally, a closed-form analytical expression is developed to estimate the input impedance of lossy power-return plane structures employed in embedded capacitance boards.

11/3,AB/53 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01/06/2003

01851801 AADAAI3025507
Nonlinear stress analysis of electronic packages
Author: Peng, Yuchun
Degree: Ph.D.
Year: 2001
Corporate Source/Institution: University of Arkansas (0011)
Source: VOLUME 62/09-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 4197. 148 PAGES
ISBN: 0-493-36970-8

To ensure good performance of electronic packages and assemblies, the material behaviors in a package or assembly have to be investigated during both the assembling and the operating stage. The material behavior can be studied using experimental approaches, which are time consuming and expensive. Compared to experimental approaches, computer models cost less. The rapid advances in packaging analysis capabilities enable researchers to analyze and solve complex problems using a number of available general-purpose computer programs. In the current work, the in-house finite element model, UASTRESS, is developed for this purpose. The UASTRESS is applied to compute the critical stress in two diamond-based assemblies and a SLIM/SHOCC package.

In this work, nonlinear finite element analysis is used to compute the critical stresses in two packages named ringframe and leadframe. Results confirm the experimental observation that the ringframe cracks during assembly. The leadframe package is numerically predicted to survive, in agreement with experiments, only if the plastic effect of Nickel is considered in addition to the plastic and creep effect of Cusil. The effects of considering elastic, elasto-plastic and elasto-plastic and creep on maximum stresses are compared in the two packages.

For the SLIM/SHOCC package, in the construction of flip chip BGAs on Multichip Modules (MCMs), the difference in coefficient of thermal expansion (CTE) between silicon chip, the BGA on MCM substrate, and the underlying **FR4 motherboard** is a significant factor in overall reliability. With flip chip underfill, the chip-to-substrate interface is strengthened significantly, resulting in less of a need for a substrate with a CTE match to silicon. Indeed, with the advent of CSP-like solder ball pitches of 0.5mm, the substrate-to-board interface can become critical if there is a significant CTE-mismatch between substrate and board.

Both the Single Level Integrated Module (SLIM) (Georgia Tech Packaging Research Center), being developed by the Georgia Tech Packaging Research Center (PRC) and Seamless High off-Chip Connectivity (SHOCC) (Dibbs et al., 1997), developed by an industrial consortium including the University of Arkansas High Density Electronic Center (HiDEC), incorporate a chip/substrate/board hierarchy with flip chips and solder ball BGA attachment.

In the present work, the resulting structure is considered for thermal stress analysis using finite element methods. The objective is to choose optimum materials in the 2<super>nd</super> and 3<super>rd</super> layer from the top so that the package survives due to thermal stresses. Three-dimensional linear elastic and viscoplastic analysis is done to investigate reliability.

11/3,AB/54 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

02297597 INSIDE CONFERENCE ITEM ID: CN024067376
Reliable Flip Chip on Flex and Flex on **FR4** Applications
Kulojaervi, K.; Kivilahti, J.

01/06/2003

CONFERENCE: Recent progress in printed circuit board technology-Conference
P: 20
Berlin, Fraunhofer-Institute IZM, 1997
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE LOCATION: Berlin
CONFERENCE DATE: Jan 1997 (199701) (199701)

11/3,AB/55 (Item 2 from file: 65)
DIALOG(R)File 65:Inside Conferences

02297580 INSIDE CONFERENCE ITEM ID: CN024067201
PERL -A **FR4** Based Micro Via Technology
Olbrich, W.
CONFERENCE: Recent progress in printed circuit board technology-Conference
P: 3
Berlin, Fraunhofer-Institute IZM, 1997
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE LOCATION: Berlin
CONFERENCE DATE: Jan 1997 (199701) (199701)

11/3,AB/56 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04794616 JICST ACCESSION NUMBER: 01A0221675 FILE SEGMENT: JICST-E
Evaluation of decoupling circuits by a miniature magnetic field probe with multilayered glass ceramic substrate.
TAMAKI NAOYA (1); MASUDA NORIO (1); ISHIZAKA KAZUYOSHI (2)
(1) Nec Seisangiken Emcgise; (2) Nihondenkishinkugarasu
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 2000, VOL.100,NO.446(EMCJ2000 91-100), PAGE.7-12, FIG.8, REF.7
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.75 621.391.8.08
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A miniature shielded loop probe for measurement of magnetic fields near LSI packages and printed **circuit board**(PCB) has been developed. This probe is designed based on a multilayered glass ceramic substrate, and achieves spatial resolution of 250.MU.m, which is 4 times greater than that of previous one using **FR4**-PCB. Improving a transitional structure between a coaxial cable and a strip line connected to the loop enabled to obtain the output which is proportional to frequency in.the range below 3GHz. The effectiveness of a decoupling capacitor connected to power supply terminal of LSI is evaluated by measurement of RF currents flowing on both LSI-side trace and power supply-side trace to the decoupling capacitor. (author abst.)

11/3,AB/57 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

2269715 H.W. WILSON RECORD NUMBER: BAST00073990

01/06/2003

Is **FR4** running out of gas?
Jorgenson, Chris;
Electronic Engineering v. 72 no886 (Nov. 2000) p. 85-8
DOCUMENT TYPE: Feature Article ISSN: 0013-4902

ABSTRACT: Part of a special section on printed **circuit board** design. The future of the **FR4** in the printed-**circuit board** industry is discussed. New technology requires higher-performance properties for **FR4** and 100 percent difunctional epoxy systems are not capable of meeting these requirements. **FR4** is essentially a woven glass impregnated with epoxy resin, and the epoxy resin has a strong impact on the material properties and application. The epoxy types used in **FR4** are split into 3 basic groups; multifunctional, high temperature, and high performance. The most recent challenge to **FR4** is how it can be manufactured for OEMs that require halogen-free materials.

11/3,AB/58 (Item 2 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1766144 H.W. WILSON RECORD NUMBER: BAST98007934
Compact plotter cuts prototype circuit boards
AUGMENTED TITLE: ProtoMat 91s/Vs from Laser & Electronics GmbH
Microwaves & RF v. 36 (Dec. '97) p. 258
DOCUMENT TYPE: Product Evaluation ISSN: 0745-2993

ABSTRACT: A review of ProtoMat 91s/VS, the latest **circuit-board** prototyping tool from LPKF Laser & Electronics GmbH of Garbsen, Germany, is presented. This **circuit-board** plotter produces prototype microwave circuit boards in less than 15 minutes, without chemical etching. The ProtoMat 91s/VS can be used with FR3 and **FR4** **circuit-board** materials in addition to all standard microwave soft boards.

11/3,AB/59 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15591678 PASCAL No.: 02-0293417
Thick film ceramic capacitors and resistors inside printed circuit boards
Microelectronics : Baltimore MD, 9-11 October 2001
BORLAND William; FELTEN John J
DuPont iTechnologies, 14 T.W. Alexander Drive, P.O. Box 13999, Research Triangle Park, NC 27709-3999, United States
International Society for Optical Engineering, Bellingham WA, United States
International symposium on microelectronics (Baltimore MD USA) 2001-10-09
Journal: SPIE proceedings series, 2001, 4587 452-457
Language: English
The high level of current interest in embedded passives in printed circuit boards is driven by the tremendous pressure to pack more circuitry into smaller spaces. However, adoption has been limited, partly due to design, prototyping and infrastructure issues, but mainly due to the lack of component density, stability and tolerances necessary for widespread replacement of discretes. Thick film ceramic capacitors and resistors are the technology ofchoice for most passive devices due to performance, stability, tolerances and availability in many sizes and grades. The focus

of this work has been to develop a process and materials to reliably incorporate thick film ceramic resistors and capacitors inside printed wiring boards, thereby providing options not previously available. The resistor materials are based on standard nitrogen firing thick film pastes that have been used in automotive applications for 15 years. Sheet resistivities range from 10 ohms/square to 10 K ohms/square. The capacitor material is a nitrogen-firing barium titanate composition. The dielectric constant is > 1000, has X7R characteristics, and yields capacitance densities of 150 nF per square inch. The compositions are printed and fired on a conditioned copper foil using a standard nitrogen thick film furnace at 900 Degree C. This is followed by lamination of the copper foil, components face down, to an **FR4** board using a standard pre-preg. Photoresist is applied to the copper and the remaining steps - expose, develop, etch and strip - are carried out under conventional PWB processing. The result is copper circuitry with ceramic components inside an **FR4** matrix. This inner layer can then be incorporated inside a multilayer PWB. This paper describes the process, presents the performance, and discusses preliminary design guidelines for the embedded passives.

11/3,AB/60 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

15204170 PASCAL No.: 01-0369696
At last! True printed circuits on organic substrates- using a polymer/metal material to print solderable conductors
IMAPS 2000 : international symposium on microelectronics : Boston MA, 20-22 September 2000
LOWRIE David J J; CHOWDHARY Balvinder; FIRMSTONE Mike G; CRAIG Hugh
Multicolore Solders Ltd, Kelsey House, Wood Lane End Hemel Hempstead HP24RQ, United Kingdom; Multicore Solders Ltd., Unknown; SVT Inc USA, United States
International Society for Optical Engineering, Bellingham WA, United States
International symposium on microelectronics (Boston MA USA) 2000-09-18
Journal: SPIE proceedings series, 2000, 4339 832-835
Language: English
The advantages of being able to screen print circuits on ceramic materials have long been known and now a material exists that allows solderable conductors to be printed and fired' on organic substrates such as **FR4** . The material is highly environmentally friendly eliminating the need for conventional subtractive processing and its associated environmentally unfriendly effluent. The amount of lead in the final product is also greatly reduced and in some cases eliminated entirely. Processing of the material is also simple with only a screen printer, oven and reflow system required The material described in the paper forms an adhesive joint to the board surface and a true metallurgical joint to any solderable surface e.g. components or existing copper tracks thus allowing its use not only as a circuitisation material but also as a conductive adhesive. The internal continuous metal structure results in very high conductivity and power handling capability The paper will describe the structure and chemistry of the material including the breakthrough, which enables high adhesion and excellent solderability in the same material. The paper will further describe how it is now possible to produce circuits and attach components with only one 'reflow' operation. The use of the material in the build up of multilayer boards and the possibility to co-fire several layers will also be discussed Finally, reliability data showing how the material is relatively unaffected by standard environmental stress regimes

and conforms to industry and Bellcore standards for surface contamination, electromigration and surface insulation resistance.

11/3,AB/61 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

14441076 PASCAL No.: 00-0099403
Effect of PCB thermal conductivity on the operating temperature of an SO-8 package in a natural convection environment : Experimental measurement versus numerical prediction
International workshop on thermal investigations of ICs and microstructures : Rome, 03-06 October 1999
LOHAN J; TIILIKKA P; RODGERS P; FAGER C M; RANTALA J
Nokia Research Center, P.O. Box 407, NOKIA GROUP, 00045, Finland; Department of Mechanical & Aeronautical Engineering, University of Limerick , Limerick, Ireland
Institut national polytechnique de Grenoble. Techniques de l'informatique et de la microelectronique pour l'architecture d'ordinateurs, Grenoble, France.; Technical University of Budapest. Department of Electron Devices, Hungary.
THERMINIC : international workshop on thermal investigations of ICs and microstructures, 5 (Rome ITA) 1999-10-03
1999 207-213
Language: English
The steady state thermal performance of an isolated SO-8 package is experimentally characterised on five thermal test Printed Circuit Boards (PCBs) and the results compared against corresponding numerical predictions. The study includes the low and high conductivity JEDEC standard, **FR4** test PCBs and typical application boards. With each PCB displaying a different internal structure and effective thermal conductivity, this study highlights the sensitivity of component operating temperature to the PCB, provides benchmark data for validating numerical models, and helps one assess the applicability of standard junction-to-ambient thermal resistance (theta ja) data for design purposes on non-standard PCBs. Measurements of junction temperature and component-PCB surface temperature distributions were used to identify the most appropriate modelling methodology for both the component and the PCB.

11/3,AB/62 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal

14439156 PASCAL No.: 00-0097388
Impact of convective environment on the distribution of heat transfer from three electronic component package types : Operating on single- and multi-component printed Circuit boards
International workshop on thermal investigations of ICs and microstructures : Rome, 03-06 October 1999
RODGERS P; LOHAN J; EVELOY V; FAGER C M
Department of Mechanical & Aeronautical Engineering, University of Limerick, Limerick, Ireland; Nokia Research Center, P.O. Box 407, NOKIA GROUP, 00045, Finland; Nokia Telecommunications, Professional Mobile Radio, P.O. BOX 380, NOKIA GROUP, 00045 , Finland
Institut national polytechnique de Grenoble. Techniques de l'informatique

et de la microelectronique pour l'architecture d'ordinateurs, Grenoble, France.; Technical University of Budapest. Department of Electron Devices, Hungary.

THERMINIC : international workshop on thermal investigations of ICs and microstructures, 5 (Rome ITA) 1999-10-03
1999 214-220
Language: English

Numerical analysis is used to investigate the sensitivity of component heat transfer to convective environment, both natural and forced, component position relative to the PCB's (Printed **Circuit Board**) leading edge, impact of upstream aerodynamic disturbance, and the representation of PCB **FR4** thermal conductivity. All numerical models used were validated in previously reported studies for the prediction of both junction temperature and component-PCB surface temperature profiles (1-4). This analysis is now extended to quantify the significance of the listed variables by analysing qualitative descriptions of the fluid flow fields and predicted component energy balances, which yields new insights of the heat transfer processes involved and sources of numerical error.

01/06/2003

18/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7471000 INSPEC Abstract Number: B2003-01-1350H-028
Title: Integrated RF architectures in fully-organic SOP technology
Author(s): Davis, M.F.; Sutono, A.; Sang-Woong Yoon; Mandal, S.; Bushyager, M.; Chang-Ho Lee; Lim, K.; Pinel, S.; Maeng, M.; Obatoyinbo, A.; Chakraborty, S.; Laskar, J.; Tentzeris, E.M.; Nonaka, T.; Tummala, R.R.
Author Affiliation: Sch. of Electr. & Comput. Eng., Georgia Inst. of Technol., Atlanta, GA, USA
Journal: IEEE Transactions on Advanced Packaging vol.25, no.2 p. 136-42
Publisher: IEEE,
Publication Date: May 2002 Country of Publication: USA
CODEN: ITAPFZ ISSN: 1521-3323
SICI: 1521-3323(200205)25:2L.136:IAFO;1-D
Material Identity Number: H273-2002-003
U.S. Copyright Clearance Center Code: 1521-3323/02/$17.00
Language: English
Abstract: Future wireless communications systems require better performance, lower cost, and compact RF front-end footprint. The RF front-end module development and its level of integration are, thus, continuous challenges. In most of the presently used microwave integrated circuit technologies, it is difficult to integrate the passives efficiently with required quality. Another critical obstacle in the design of **passive components** , which occupy the highest percentage of integrated circuit and **circuit board** real estate, includes the effort to reduce the module size. These issues can be addressed with **multilayer** substrate technology. A **multilayer** organic (MLO)-based process offers the potential as the next generation technology of choice for electronic packaging. It uses a cost effective process, while offering design flexibility and optimized integration due to its **multilayer** topology. We present the design, model, and measurement data of RF-microwave **multilayer** transitions and integrated passives implemented in a MLO system on package (SOP) technology. Compact, high Q inductors, and embedded filter designs for wireless module applications are demonstrated for the first time in this technology.
Subfile: B

18/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6602584 INSPEC Abstract Number: B2000-07-2210D-024
Title: Step-by-step SMT. IV. Printing
Author(s): Godlin, R.; Johnson, A.
Author Affiliation: Speedline MPM, Franklin, MA, USA
Journal: Surface Mount Technology vol.14, no.4 p.73-4
Publisher: PennWell Publishing,
Publication Date: April 2000 Country of Publication: USA
CODEN: SMTEEL ISSN: 0893-3588
SICI: 0893-3588(200004)14:4L.73:SSP;1-D
Material Identity Number: N547-2000-006
Language: English
Abstract: Products requiring flexible circuits, such as smart cards and RFID tags, have fueled the growing use of nonrigid PCBs by the electronics industry. Some components, such as the mu BGA and other CSPs, are built

using a flexible tape, while other circuits are built on ceramics either in the green (unfired) or rigid format. Flip chips are usually completely processed in the wafer format as in the emerging technology of wafer scale packaging (WSP). Printing on nonprinted **circuit board** (PCB) substrates requires special abilities and printer adaptations. The materials' particular properties, such as fragility, flexibility, lightness, and thinness down to 0.002", present special handling challenges. Additionally, very fast printing speeds may be required for specific substrate printing. Typical print materials include: **conductive**, dielectric and **resistive** pastes or inks; adhesive epoxies; conductive epoxies; solder paste (on metal foil circuits); polymeric materials such as polymer thick films; silicones; and frit (glass) paste.
Subfile: B

18/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6383895 INSPEC Abstract Number: B1999-12-2120-002
Title: Metal-containing polymer-based composites for resistor and thermistor applications
Author(s): Xiaomei Xi; Brandt, L.; Matijasevic, G.; Fu, S.; Gandhi, P.; Baxter, D.; Owings, G.
Author Affiliation: Ormet Corp., Carlsbad, CA, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3582 p.453-8
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3582L.453:MCPB;1-M
Material Identity Number: C574-1999-173
Conference Title: 1998 International Symposium on Microelectronics
Conference Sponsor: SPIE; IMAPS
Conference Date: 1-4 Nov. 1998 Conference Location: San Diego, CA, USA
Language: English
Abstract: Embedding **passive components** into **multilayer** structures is one of the latest approaches to increasing "silicon" density on circuit boards. While embedded **passive components** made with thin film and ceramic thick film technologies have been developed, these are generally not applicable to polymer-based **circuit board** substrates. Consequently, polymer thick films, which are compatible with printed wiring boards, are being developed as an inexpensive path to integrated **passive components** . This paper introduces a novel approach to polymer-based resistor materials using a partially sintered metallic network instead of the particle-to-particle connections seen in typical carbon-filled resistor materials. By alloying to the copper pads, the resistor material provides a stable electrical junction, while the interpenetrating polymer provides adhesion to a variety of polymer and metal surfaces. The resistor material has been deposited by a number of different methods including stenciling, screen-printing, and filling of photo-patterned dielectrics. Test results obtained to date with these resistor materials on various substrates are presented. In order to demonstrate the feasibility of an embedded additive **multilayer circuit board** , the photodefining technology was also used to pattern resistors, capacitors and conductive circuitry. Along with the resistor materials, which have a relatively low temperature coefficient of resistance (TCR), polymer-metal thermistor materials with a high TCR have

also been developed.
Subfile: B
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18/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6307576 INSPEC Abstract Number: B1999-09-2120-002
Title: Planar resistor technology
Author(s): Brandler, D.
Author Affiliation: Ohmega Technol. Inc., Culver City, CA, USA
Conference Title: Proceedings of the Technical Program. NEPCON West '97. Conference Part vol.3 p.1614-19 vol.3
Publisher: Reed Exhibition, Norwalk, CT, USA
Publication Date: 1997 Country of Publication: USA 3 vol. 1754 pp.
Material Identity Number: XX-1999-01551
Conference Title: Proceedings of NEPCON West '97
Conference Date: 23-27 Feb. 1997 Conference Location: Anaheim, CA, USA
Language: English
Abstract: Electronics Manufacturing Technology Roadmaps suggest that the continuing trend toward increased density and complexity in printed circuit boards is driving a shift to integral **passive components** as an alternative to surface mounted discrete **passive components**. Integral **passive components** are resistors, capacitors or inductors that are incorporated within an interconnecting substrate. The focus of this paper is on Planar Resistor Technology (PRT). Planar Resistor Technology enables the generation of thin film buried resistors for standard **multilayer** printed circuit boards. Standard CAD systems are used to design planar resistors. The resistors are incorporated into the PCB layout usually into existing layers. CAD systems with component libraries that include planar resistor footprints speed the design process. Design trends toward higher resistor values, tighter tolerances and smaller resistor footprints increase the required sheet resistivity. Newer PRT materials are more chemically resistant, providing greater stability for tighter tolerances. Improved CAD systems provide resistor values and locations to reduce editing at the CAM station. New software allow Resistor Test Files to be used in conjunction with standard net lists for rapid testing using conventional bare board test equipment. Integral **passive components** reduce assembly time, rework and testing, enabling rapid prototyping and reduced time to market.
Subfile: B

18/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6265059 INSPEC Abstract Number: B1999-07-2210D-031, C1999-07-7410D-058
Title: The implementation of integral **passive component** technology: a case study
Author(s): Brandler, D.
Conference Title: 18th Capacitor and Resistor Technology Symposium. CARTS '98 p.67-76
Publisher: Components Technol. Inst, Huntsville, AL, USA
Publication Date: 1998 Country of Publication: USA 266 pp.
Material Identity Number: XX-1997-01940
Conference Title: Proceedings of CARTS-USA 96
Conference Sponsor: Components Technol. Inst.; IEEE; Int. Microelectron.

& Packaging Soc
Conference Date: 9-13 March 1998 Conference Location: Huntington Beach, CA, USA
Language: English
Abstract: This paper documents steps taken by a medium volume printed **circuit board** manufacturer as they implement the equipment, processes and methods required for planar resistors. The focus is on buried resistors in high density **multilayer** PCBs for high speed telecommunication systems. A short overview of integral **passive component** technology is presented. Modification of the PCB manufacturer's existing facilities and added capital equipment requirements are discussed. The paper follows progress from the receipt of the design data to the delivery of production boards. Topics covered include: (1) the implementation of special processes and procedures; (2) **passive component** CAD/CAM software and data requirements; (3) electrical testing of inner layer and finished boards. The results of a process capability study are presented with a comparison between test vehicle and production boards.
Subfile: B C

18/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

6020511 INSPEC Abstract Number: B9810-2210D-041
Title: New materials for embedded **passive components**
Author(s): Brandt, L.; Xi, X.; Baxter, D.; Owings, G.; Fu, S.; Matijasevic, G.; Gandhi, P.
Author Affiliation: Ormet Corp., Carlsbad, CA, USA
Conference Title: Pan Pacific Microelectronics Symposium. Proceedings of the Technical Program p.195-9
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 1998. Country of Publication: USA. 508 pp.
Material Identity Number: XX98-00364
Conference Title: Proceedings of Pan Pacific Microelectronics Symposium
Conference Sponsor: Surface Mount Technol. Assoc.; Int. Microelectron. & Packaging Soc.; Semicond. Equipment & Mater. Int
Conference Date: 10-13 Feb. 1998 Conference Location: Kona, HI, USA
Language: English
Abstract: Freeing up expensive **circuit board** real estate is the major drive for embedding **passive components** into **multilayer** structures. Three approaches are currently being investigated by several industry consortia: thin film, ceramic thick film and polymer thick film. Of these, the polymer thick film approach is the most inexpensive and most appropriate for laminate **multilayer** structures. However, this technology is also considerably less `mature' than the other two approaches. Novel polymer based materials for embedded resistors, capacitors and inductors have been developed to address this need. Vertical and horizontal electrical interconnects, contact pads and electrodes can be formed with highly conductive, sinterable inks. Apart from the materials, engineering problems must be dealt with. An example of how to integrate embedded **passive components** with a fully additive **multilayering** technology is shown with a simple oscillator circuit. The approach uses a thin metal substrate and a permanent, photodefinable polymeric insulator to control component tolerances and maintain coplanarity for component attachment.
Subfile: B

01/06/2003

18/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

5362738 INSPEC Abstract Number: B9610-2210B-035
Title: PCMCIA design pitfalls
Author(s): Roach, L.B.
Author Affiliation: AT&T Bell Labs., Princeton, NJ, USA
Conference Title: SMI Surface Mount International. Advanced Electronics Manufactuting Technologies. Proceedings of the Technical Program p. 1021-5
Publisher: SMTA, Edina, MN, USA
Publication Date: 1995 Country of Publication: USA 1082 pp.
Material Identity Number: XX96-01150
Conference Title: Proceedings of Surface Mount International Conference
Conference Date: 29-31 Aug. 1995 Conference Location: San Jose, CA, USA
Language: English
Abstract: At the start of AT&T's project to build a data card, there were a lot of major hurdles to overcome. The PCMCIA standard was very young and unstable at that stage. There were no available PCMCIA Type II frames or covers, and few connector manufacturers, and there was no thin FR-4 **multilayer** printed **circuit board** manufacturing (0.016 mil thick, 6 layers) capability. The microprocessor used was only available in a CQFP package (ceramic quad flat pack) which is 0.170 mils high, with a maximum allowable height of 0.072 mils high from the PCB Cu surface to the inside of the covers. The assembly of this technology was a very difficult task, with double sided IR reflow of active and **passive components** . These were just a few of the pitfalls encountered in our first attempt at PCMCIA cards. This paper explains how AT&T overcame the PCMCIA design pitfalls.
Subfile: B

18/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

5322710 INSPEC Abstract Number: B9608-1350H-057
Title: Development of a new line of low cost microwave components using print and fire technologies
Author(s): Ralph, L.E.
Author Affiliation: R.F. Prime Corp., Sacramento, CA, USA
Conference Title: Conference Proceedings. RF Expo East 1994. The Wireless Show That Goes the Distance p.11-16
Publisher: Argus Business, Englewood, CO, USA
Publication Date: 1994 Country of Publication: USA 218 pp.
Material Identity Number: XX95-00468
Conference Title: Proceedings RF Expo East
Conference Sponsor: RF Design Magazine
Conference Date: 15-17 Nov. 1994 Conference Location: Orlando, FL, USA
Language: English
Abstract: Over the past few years, many high performance **passive components** have been developed for the military/commercial marketplace. Designs using duroid structures allowed lower cost, but were not applicable to miniaturization or surface mounting. Products developed for surface mount using thin film microstrip are expensive, and usually rigidly mounted to the printed **circuit board**. A new line of products has been developed by combining an old technology with new design

approaches. Thick film technologies have evolved from simple lines and resistors, to advanced **multilayer** structures implementing near fine line capability. Yet the lower cost inherent in a screen print and fire operation has been maintained. It was because of these advances that RF Prime began developing a microwave thick film technology. The resulting process is known as Blue Cell technology. This technology goes beyond simple balun structures, and allows the implementation of low inductance capacitors, inductors, and unique resonator structures. The all printed structure provides repeatability closer to that of semiconductor processing than standard hybrid assembly.
Subfile: B

18/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

04051721 INSPEC Abstract Number: B9202-2210D-057
Title: Copper polymer thick film for high density and multilayer interconnects
Author(s): Russell, K.
Author Affiliation: MINICO PTF Technol. Center, Congers, NY, USA
Journal: Electronic Packaging and Production vol.31, no.9 p.58-61, 63
Publication Date: Sept. 1991 Country of Publication: USA
CODEN: ELPPA5 ISSN: 0013-4945
Language: English
Abstract: Polymer thick film (PTF) **conductive, resistive** and dielectric inks increase speed and efficiency for printed **circuit board** production. A new PTF has advanced PTFs to the point where the low-cost additive process is acceptable for producing high density and multilayer circuits. PTF technology has been widely accepted for providing dielectric and resistor systems in recent years. But, its growth has been limited by the performance of conductive PTF materials. The copper PTF overcomes previous limitations and eliminates the need for conductive adhesives. It also allows manufacturers who have been using the subtractive process with copper clad boards to investigate an alternative process which avoids waste management issues involving heavy metal disposal. The performance characteristics of PTF systems using this new copper product in PCBs produced both with IR and vapor phase curing systems are discussed.
Subfile: B

18/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

02948589 INSPEC Abstract Number: B87053012
Title: The construction and manufacture of flexible circuit boards
Author(s): Kober, J.
Journal: EEE no.7 p.43-51
Publication Date: 31 March 1987 Country of Publication: West Germany
CODEN: EESTEL ISSN: 0174-7452
Language: German
Abstract: In conjunction with flat cables and rigid printed circuits, flexible circuit boards, which save space and weight, offer the possibility of new connection techniques. The continuous development of flexible circuit boards has changed them from a mere means of connection to a combination of connectors with means of supporting active and **passive components** . Electrical equipment can thus be further miniaturised

and the applications of flexible circuit boards can be further extended. To manufacture such equipment economically the correct flexible material and the appropriate production techniques must be used. To facilitate the correct method of manufacture some five different applications are mentioned. Various types of flexible **circuit board** are mentioned: one and two sided flexible CB; **multilayer** CB; rigid/flexible CB. Various basic materials, types of foil and bonding materials are detailed and methods of manufacture are discussed. In conclusion, the author deals with electric testing, altering dimensions during the manufacturing process and means of ensuring satisfactory manufacture.
Subfile: B

18/3,AB/11 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1362763 H.W. WILSON RECORD NUMBER: BAST96036246
Multilayer PTFE circuits for RF applications
Jandzinski, David A; Stafford, John W; Huang, Phil M
Microwave Journal v. 39 (May '96) p. 264+
DOCUMENT TYPE: Feature Article ISSN: 0192-6225

ABSTRACT: The writers discuss new filled polytetrafluoroethylene (PTFE) materials that may be used to achieve high-frequency printed circuit performance at a relatively low cost. As a result of the low loss factor and stable dielectric constant of these filled printed **circuit board** laminates, they are ideal for microwave and radio-frequency circuits. The writers examine the electrical design and process development issues associated with multiple-layer filled PTFE material and conclude that multiple-layer filled PTFE materials can be employed to produce other building blocks, such as transformers, diplexers, and other **passive components**.

18/3,AB/12 (Item 2 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1169065 H.W. WILSON RECORD NUMBER: BAST94037663
The use of multi-chip modules in safety critical systems
Roughton, Mike; Hinde, Gary
Electronic Engineering v. 66 (May '94) p. 35-6+
DOCUMENT TYPE: Feature Article ISSN: 0013-4902

ABSTRACT: The design and manufacture of a multi-chip module (MCM) for a safety critical aero-engine application are described. A generic full authority digital engine control system for medium to large aero-engines was designed. Initially, the system was designed as a conventional printed **circuit board**. However, MCM technology was subsequently employed in order to achieve the current objectives of reduced size, weight, and component count and increased reliability at a competitive price. The space saving over a standard plated through hole printed **circuit board** was better than a factor of 4; in addition, 148 **passive components** were eliminated.

18/3,AB/13 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15488184 PASCAL No.: 02-0183245
Electrical behavior of decoupling capacitors embedded in **multilayered** PCBs : Recent Advances in EMC of Printed Circuit Boards
MADOU An; MARTENS Luc
Department of Information Technology (INTEC), IMEC-Ghent University, Ghent 9000, Belgium
Journal: IEEE transactions on electromagnetic compatibility, 2001, 43 (4) 549-556
Language: English
In this paper, we describe the modeling of prototype capacitors embedded in **multilayered** printed circuit boards. We present the design of these devices. We also report measurement and characterization results. The emphasize is on the modeling of via hole connections to the embedded capacitor, not on the technology of buried capacitors in se. Several designs have been compared with respect to their electrical behavior. In particular, several via hole configurations have been studied, because they are the main cause of parasitic behavior. With these buried capacitors, we obtained a reduction of the parasitic inductance of 80% compared to an equivalent discrete capacitor. This work has been carried out under a European Brite-EuRAM funded project COMPRISE (BE 96-3371). The objective of this project was to develop new materials and manufacture processes to embed **passive components** (R, L, and C) within printed wiring structures fabricated from laminate materials. This technology enables the manufacture of space efficient and radio frequency (RF) optimal performing types of modules or board assemblies particularly suited to the market domain of portable and handheld communication and information technology products.

18/3,AB/14 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

15197203 PASCAL No.: 01-0362440
New feasibilities for **multilayer** Boards polymer-thick-film Technology on silicone polymer substrates
IMAPS 2000 : international symposium on microelectronics : Boston MA, 20-22 September 2000
BISCHOFF Gernot; WINKLER Gert; LANDECK Hubert
Ilmenau Technical University, Faculty of Electrical Engineering and Information Technique, Electronics Technology Group, P.O. Box 10 05 65, 98684 Ilmenau, Germany; KEW Konzeptentwicklung GmbH, Klosterstrasse 13, 96317 Kronach, Germany
International Society for Optical Engineering, Bellingham WA, United States
International symposium on microelectronics (Boston MA USA) 2000-09-18
Journal: SPIE proceedings series, 2000, 4339 346-350
Language: English
Today many electronic devices are designed and produced with a multiplicity of fabrication techniques. The spectrum ranges from standard Printed Circuit Boards and conventional thick film technology on ceramic substrates to special applications i.e. LTCC with chip on board. The materials used and the fabrication steps often contain environmentally harmful substances. Many materials are very expensive, too. Therefore the disposal of discarded goods with a mix of many various materials is a problem which is becoming an important criterion in marketing products. For an environmentally friendly low cost application it is necessary to eliminate harmful substances, reduce the variety of materials and

fabrication techniques, and increase the reliability. Polymer-Thick-Film Technology (PTF) on silicone polymer substrate is a very interesting and novel technology for interconnection and passive integration. PTF on silicone uses heatconducting foils with a copper cladding as base material for printed circuit boards. The pattern may take be formed by an etching process and/or by screen printing of polymeric inks. The excellent thermal conductivity and the good flexibility allow the designer to construct high power modules and three dimensional packages with integrated **passive components** . Another advantage is the possibility to utilize these materials and technologies to manufacture **multilayer** boards. This paper intends to describe the feasibility to build three dimensional components (**multilayer** coils) and **multilayer** boards by using PTF on silicone substrates. It demonstrates a new solution of **multilayer** technology for Polymer Boards.

18/3,AB/15 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

14688504 PASCAL No.: 00-0363580
Embedded **passive components** and PCB size : thermal effects
STUBBS D M; PULKO S H; WILKINSON A J; WILSON B; CHRISTIAENS F; ALLAERT K
The University of Hull, Hull, United Kingdom; Department of Electrical Engineering and Electronics, UMIST, Manchester, United Kingdom; Alcatel Bell NV, Antwerpen, Belgium
Journal: Microelectronics international, 2000, 17 (2) 7-10
Language: English
The embedding of **passive components** such as resistors, capacitors and inductors within printed circuit boards (PCBs) is motivated, to a large extent, by the desire for increased miniaturisation of electronic goods. However, resistors and, to a lesser extent, inductors are heat generating devices, and the temperature developed within PCBs as the result of the operation of embedded passives is a significant aspect of the design of a **multilayer** PCB. Here we investigate, by simulation, temperature fields associated with operation of embedded resistors. It is shown that for board dimensions less than 2cm x 2cm temperatures achieved are higher than those associated with larger boards having identical structures and identical resistor heat generation. Detailed simulations are used to investigate the sensitivity of the temperature rises associated with embedded resistors to copper track coverage and to thermal coupling of the PCB to ambient on its upper and lower surfaces. The implications of these findings are discussed both in the context of the design of real PCBs and in the context of thermal simulation.

18/3,AB/16 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal

14461785 PASCAL No.: 00-0121676
Miniaturized cofired integrated passive filter networks
IMAPS : international symposium on microelectronics : Chicago IL, 26-28 October 1999
RITTER A; SMITH B; STRAWHORNE M; HEISTAND R II
AVX Advanced Product and Technology Center, 2200 AVX Drive, Myrtle Beach, SC, 29577, United States; AVX Limited, Hillman's Way, Coleraine, Northern

Ireland, BT52 2DA, United Kingdom
International Society for Optical Engineering, Bellingham WA, United States.; International Microelectronics and Packaging Society, United States.
International symposium on microelectronics (Chicago IL USA) 1999-10-26
Journal: SPIE proceedings series, 1999, 3906 658-663
Language: English
Cofired buried resistors are used to make an integrated series resistor-capacitor **multilayer** device, -Z- Chip SUP < SUP T SUP M >, with an integral resistive electrode design. Introduction of internal conductors in conjunction with the buried resistive electrodes allows higher degrees of integration in 2-port devices. Designs and performance data for volumetrically efficient low pass filter arrays and multi-value resistor-capacitor networks are examples of a manufacturing approach that evolved from **multilayer** ceramic capacitor technology incorporating low temperature cofired materials. A **circuit board** -level component density figure of merit for comparing discrete and integrated devices is discussed.

18/3,AB/17 (Item 5 from file: 144)
DIALOG(R)File 144:Pascal

14460563 PASCAL No.: 00-0120246
Embedded **passive components** for printed-circuit boards
IMAPS : international symposium on microelectronics : Chicago IL, 26-28 October 1999
WU L K; TSENG B C; LIAO L C
Department of Communication Engineering, National Chiao Tung University 1001 Ta Hsueh Rd., Hsinchu, 310 , Taiwan; Computer & Communications Research Laboratories, Industrial Technology Research Institute S200 CCL/ITRI Bldg. 14, 195-11 Sec. 4, Chung Hsing Rd. Chutung, Hsinchu, 310, Taiwan
International Society for Optical Engineering, Bellingham WA, United States.; International Microelectronics and Packaging Society, United States.
International symposium on microelectronics (Chicago IL USA) 1999-10-26
Journal: SPIE proceedings series, 1999, 3906 499-504
Language: English
Demand for significant size reduction of circuitry used to build various portable products has increased rapidly in recent years. While significant strides have been made in the integration of active components, only little progress has been made in the integration ofpassive components. Together with the increasing circuit complexities to meet the increasing demand on a product's functionality, number of **passive components** used in a typical portable product has increased significantly in recent years and may account for 70-80% of the total part count. The embedded passives technology that was developed recently is aimed at integrating various **passive components** at the printed-**circuit board** level. By integrating these passives, manufacturers may obtain the following advantages: (1) a dramatic reduction in the overall part count, (2) improved wireability due to the elimination of vias, (3) improved reliability due to the elimination of solder joints, and (4) improved frequency response due to the elimination of parasitic inductance.

01/06/2003

18/3,AB/18 (Item 6 from file: 144)
DIALOG(R)File 144:Pascal

14460468 PASCAL No.: 00-0120143
High resolution coplanar structures on **multilayer** LTCC for applications up to 40 GHz
IMAPS : international symposium on microelectronics : Chicago IL, 26-28 October 1999
KULKE R; RITTWEGER M; SIMON W; WIEN A; WOLFF I
Institute of Mobile and Satellite Communication Techniques (IMST), Carl-Friedrich-Gauss-Strasse 2, 47475 Kamp-Lintfort, Germany
International Society for Optical Engineering, Bellingham WA, United States.; International Microelectronics and Packaging Society, United States.
International symposium on microelectronics (Chicago IL USA) 1999-10-26
Journal: SPIE proceedings series, 1999, 3906 79-83
Language: English
The announcement of photoimageable metallisation in conjunction with the conventional screen printing process supports the idea to develop **passive components** for multichip applications up to an estimated frequency limit of 40 GHz. This technique has been developed by DuPont and is called Fodel SUP (R) , which has been printed first in a postfired and later in a cofired process on the LTCC Green Tape 951. In the national supported "4M"-project, which is an abbreviation for multifunctional micro- and mm-wave modules, a 4x4-inch LTCC tile with 4 substrate layers and a great number of coplanar, microstrip and stripline test structures and circuits has been designed and fabricated. In the first technology run, the postfired test structures show higher fabrication tolerances, which result in a shift of the Fodel SUP (R) metal to the inner thickfilm layers and a higher shrinking than expected. In spite ofthese drawbacks a number of structures and circuits have been evaluated. In a second technology run, the same layout has been fabricated with a cofired Fodel metallisation. The new tiles show an improved alignment between inner and top layer as well as lower shrinking tolerances. Measured and simulated results from both technology runs will be demonstrated and evaluated. Beside the technology aspects, the focus ofthese investigations lies on the capability ofsimulation tools for **multilayer** circuits as well as on applications aspects for RF circuits up to 40 GHz.

18/3,AB/19 (Item 7 from file: 144)
DIALOG(R)File 144:Pascal

12897805 PASCAL No.: 97-0163222
Microelectronics : Minneapolis MN, 8-10 October 1996
International Society for Optical Engineering, Bellingham WA, United States.; International Society for Hybrid Microelectronics, Montgomery AL, United States.
International symposium on microelectronics (Minneapolis MN USA) 1996-10-08
Journal: SPIE proceedings series, 1996, 2920 XIII, 610 p., ill., index Non-paginated pages/foldouts
Language: English Summary Language: English

01/06/2003

18/3,AB/20 (Item 1 from file: 315)
DIALOG(R)File 315:ChemEng & Biotec Abs

495919 CEABA Accession No.: 33-10-000090 DOCUMENT TYPE: Journal
Title: Development trends for passive devices: becoming active in electrical engineering
Orig. Title: Bauelemente der Elektrotechnik: Passive sind sehr aktiv
AUTHOR: Knurhahn, P.
CORPORATE SOURCE: selbst., Muenchen, D
JOURNAL: Tech. Rundsch., Volume: 92, Issue: 21, Page(s): 40-42
CODEN: TCRUAU ISSN: 10230823
PUBLICATION DATE: 2000 (20000000)
ABSTRACT: Passive' electronic components are defined to be energy consumers in contrast to 'active' components such as signal amplifying transistors. At the moment, component costs approach zero, while mounting, soldering and testing make up for 95% of the total costs. The sub-millimetre components have to be placed exactly onto the **circuit board**, soldered safely and tested. There are three trends: miniaturisation, altered distribution of production work between producers and applicants (manufacturers of electronic devices), and new developments based on known technologies. The main revolution in the line is the integration of many **passive components** in a block, forming three-dimensional ceramic or **multi-layer circuit board** modules at the producer's site with only minor applicant handling requirements. This is exemplified by the new xenon high intensity discharge automotive lighting systems where the high voltage igniter (20,000 V) was mounted into the lamp socket housing, i.e. easy assembling for the automotive industry. Integrated modules open up new fields of application such as high frequency ceramics for television and mobile phones. All **passive component** markets have significantly grown in 2000, HF components, piezo ceramics, inductive and EMV components, resistors, and condensers, altogether from 1.45 mio. Euro in 1999 to 1.85 mio. Euro in 2000.

01/06/2003

40/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6887676 INSPEC Abstract Number: B2001-05-6250F-253
Title: Thin film passives in miniaturisation of cellular electronics
Author(s): Pohjonen, H.; Pienimaa, S.
Author Affiliation: Nokia Mobile Phones Ltd., Salo, Finland
Conference Title: 19th Capacitor and Resistor Technology Symposium. CARTS '99 p.180-5
Publisher: Components Technol. Inst, Huntsville, AL, USA
Publication Date: 1999 Country of Publication: USA xii+362 pp.
Material Identity Number: XX-2001-00448
Conference Title: 19th Capacitor and Resistor Technology Symposium. CARTS'99
Conference Sponsor: Components Technol. Inst.; IEEE - Components, Packaging, & Manuf. Technol. Soc.; IMAPS - Int. Microelectron. & Packaging Soc
Conference Date: 15-19 March 1999 Conference Location: New Orleans, LA, USA
Language: English
Abstract: Miniaturisation has been one of the drivers in portable cellular electronics during the past four years. **Passive components** take a remarkably large part of the real estate of the board assembly. In RF and IF applications in particular, these are clearly the most used components. The limited Q values of thin film passives have been considered to limit their use: Q values of 30-50 for MIM **capacitors** and thin film inductors, 8-12 on a lossy semiconductor substrate, or 30-80 when on insulating low-loss substrates like ceramic and quartz. Part of these limitations can be overcome by design optimization, enabled by accurate modeling and simulation techniques. Although novel simulation methods have been utilized, several iteration s are needed so that acceptance criteria can be met. The modules must conform to the specifications of the cellular electronics. A 50% area reduction has been demonstrated using wire bonding and thin film passive integration. An additional 25% area reduction is achieved using flip chip interconnections in cellular RF and IF functions, when compared to the functionally equivalent assembly, based on TQFP packaged ICs and SMD discretes on a printed **circuit board**.
Subfile: B

40/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6815701 INSPEC Abstract Number: B2001-02-0170J-051
Title: Fabrication of a fully integrated passive module for filter application using MCM-D compatible processes
Author(s): Bhattacharya, S.K.; Park, J.Y.; Tummala, R.R.; Allen, M.G.
Author Affiliation: Sch. of Electr. & Comput. Eng., Georgia Inst. of Technol., Atlanta, GA, USA
Journal: Journal of Materials Science: Materials in Electronics vol.11, no.6 p.455-60
Publisher: Kluwer Academic Publishers/Chapman & Hall,
Publication Date: Aug. 2000 Country of Publication: USA
CODEN: JSMEEV ISSN: 0957-4522
SICI: 0957-4522(200008)11:6L.455:FFIP;1-0
Material Identity Number: H206-2001-001

U.S. Copyright Clearance Center Code: 0957-4522/2000/$15.00
Language: English
Abstract: Integral passive is an emerging technology which is currently perceived as a possible alternative to the discrete passive technology in fulfilling the next generation packaging needs. Although discrete surface **mount passive components** (resistors, **capacitors**, and inductors) have been well characterized, the development of integral **passive components** suitable for co-integration on the board level is relatively recent. Since in some applications the number of **passive components** can exceed the number and the area of IC chips on a **circuit board** or in a package, such integration of **passive components** would be necessary to substantially eliminate part count and reduce device area. To address these issues, integration technology for passive elements in the same manner as for transistors is necessary. In addition, the fabrication sequence of all integral **passive components** should be mutually compatible for co-integration on the same substrate. In this paper, materials and fabrication issues for passive elements such as resistors (R), **capacitors** (C), and inductors (L) and the feasibility of integration of these fabricated **passive components** on glass substrates have been addressed. An active filter circuit has been selected for a case study for R, L, and C co-integration. This passive module contains eleven resistors, four **capacitors** , and four inductors, and is fabricated using MCM-D (multichip module-deposited) compatible processes. A variety of materials appropriate for fabrication of integral passives in a mutually compatible fashion were investigated, including chromium and nickel-chromium resistors, composites of high dielectric constant materials in epoxies for **capacitor** dielectrics, and composites of magnetic ferrite particles in polyimides for inductor core and shielding. The fabricated devices showed good agreement between the design values and the corresponding measured values. It is anticipated that some of these materials and fabrication processes can be implemented for the MCM-L (multichip module-laminate) compatible packaging.
Subfile: B

40/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6781819 INSPEC Abstract Number: B2001-01-2210D-022
Title: Mass reflow assembly of 0201 components
Author(s): Adriance, J.; Schake, J.
Author Affiliation: Universal Instrum. Corp., Binghamton, NY, USA
Journal: Surface Mount Technology vol.14, no.9 p.97-8, 100, 102, 104, 106
Publisher: PennWell Publishing,
Publication Date: Sept. 2000 Country of Publication: USA
CODEN: SMTEEL ISSN: 0893-3588
SICI: 0893-3588(200009)14:9L.97:MRA0;1-X
Material Identity Number: N547-2000-013
Language: English
Abstract: The need to reduce the size and weight of electronic products continues as SMT advances. Size reductions of **passive components**, coupled with improved printed **circuit board** (PCB) technology, produces smaller, lighter and higher performing end products. Extensive research and development continues to reduce the size of active packages. Smaller **passive components** enable designers to use more compact PCBs to perform a given task. Using 0603 and 0402 components, for example, has been prevalent for numerous years; these parts

can be run in high-volume applications at very high yields. More recently, 0201 components have been implemented in high-density applications. These parts are approximately one-quarter the size of 0402 components and thus could reduce assembly process robustness and yield. This article describes the results of an ongoing study to determine the impact that specific assembly and board design parameters have on assembly yield of 0201-size components in a mass reflow setting. Combining flux type and reflow environment has the greatest effect on the number of defects produced. Boards with no-clean solder paste reflowed in an air atmosphere exhibit the best yields with the highest tolerance for attachment pad dimension variation.
Subfile: B

40/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6781814 INSPEC Abstract Number: B2001-01-2210D-019
Title: 0201 technology drives process solutions [PCB design/processing]
Author(s): Lewis, B.J.; Houston, P.
Author Affiliation: Siemens EAE, Norcross, GA, USA
Journal: Surface Mount Technology vol.14, no.9 p.54-6, 58, 60
Publisher: PennWell Publishing,
Publication Date: Sept. 2000 Country of Publication: USA
CODEN: SMTEEL ISSN: 0893-3588
SICI: 0893-3588(200009)14:9L.54:0TDP;1-2
Material Identity Number: N547-2000-013
Language: English
Abstract: Ultra-small footprint passives, such as 0201 components, are a hot topic in the electronics industry. Existing as a compliment to high input/output (I/O) devices, such as chip scale packages (CSP) and flip chip technologies, these components are needed for electronic package miniaturization. Dimensions of 0.02*0.01" make these components ideal for high-density packaging when used in conjunction with other technologies. This article covers a comprehensive view of the work that has been published, highlights aspects of board design guidelines and defines process windows for printing, placement and reflow. It also covers a project investigating **circuit board** design parameters, process limitations, and process guidelines to produce a robust process window and board design layout. Project aspects are discussed and tentative data is given, but as the project is ongoing, final data compilation is yet to be published.
Subfile: B

40/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5953293 INSPEC Abstract Number: B9808-0170J-054
Title: Fully integrated passives modules for filter applications using low temperature processes
Author(s): Park, J.Y.; Bhattacharya, S.K.; Allen, M.G.
Author Affiliation: Packaging Res. Center, Georgia Inst. of Technol., Atlanta, GA, USA
Conference Title: Proceedings. 1997 International Symposium on Microelectronics (SPIE vol.3235) p.592-7
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA

Publication Date: 1997 Country of Publication: USA xvii+707 pp.
ISBN: 0 930815 50 5 Material Identity Number: XX98-00801
Conference Title: Proceedings 1997 International Symposium on Microelectronics
Conference Sponsor: IMAPS - Int. Microelectron. & Packaging Soc
Conference Date: 14-16 Oct. 1997 Conference Location: Philadelphia, PA, USA
Language: English

Abstract: Although discrete surface **mount** **passive** **components** (resistors, **capacitors** , and inductors) have been well developed, the development of integrated **passive** **components** suitable for integration with printed wiring boards is relatively recent. Since in some applications the number of **passive** **components** can exceed both the number and area of IC chips on a **circuit** **board** or in a package, such integration is desirable. To address these issues, integration technology for passive elements in the same manner as for transistors is necessary. An additional issue to be considered is that the fabrication sequences of all integrated **passive** **components** must be compatible is they are to be integrated on the same substrate. In this paper, a fully integrated passives module is presented. This passives module contains eleven resistors, four **capacitors** , and four inductors, and is fabricated using techniques which are compatible with organic substrates such as fiber-epoxy board. A variety of materials appropriate for low temperature fabrication of integrated passives in a mutually compatible fashion were investigated, including chromium and nickel-chromium resistors, composites of high dielectric constant materials in epoxies for **capacitor** dielectrics, and composites of magnetic ferrite particles in polyimides for inductor cores and shielding. The as-fabricated devices showed good agreement between the design values and the corresponding measured values.

Subfile: B

40/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

03524472 INSPEC Abstract Number: B90002559
Title: Surface **mountable** chip ferrite beads for EMI suppression
Author(s): Kuhl, T.
Author Affiliation: Murata Erie, North America Inc., Smyrna, GA, USA
Conference Title: 9th Capacitor and Resister Technology Symposium. CARTS '89 p.121-5
Publisher: Components Technol. Inst, Huntsville, AL, USA
Publication Date: 1989 Country of Publication: USA 155 pp.
Conference Sponsor: Component Technol. Inst
Conference Date: 15-16 March 1989 Conference Location: Orlando, FL, USA
Language: English

Abstract: While surface **mounting** of electronic components continues its rapid growth as the preferred method of printed **circuit** **board** assembly, manufacturers of such components are striving to produce leadless chip versions of virtually every through hole device that is currently offered in the marketplace. In the case of **passive** **components**, chip **capacitors** and resistors are relatively mature as component sizes and performances have been standardized and there are a number of vendors who can supply these high quality components. However, for this technology to truly advance, all varieties of components must be available in chip form so that assemblies are completely surface **mounted** . In response to that challenge, vendors are now producing

chip versions of many different components. Among these is the recent introduction of surface **mount** chip ferrite beads, to be used for the suppression of electromagnetic interference (EMI). These components offer excellent performance at a low cost, and are capable of withstanding today's automated assembly techniques.
Subfile: B

40/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

03108430 INSPEC Abstract Number: B88024552
Title: Electromechanical components in SMD-techniques
Author(s): Bartel, M.
Journal: Elektronik Industrie vol.18, no.11 p.16, 18, 20
Publication Date: 1987 Country of Publication: West Germany
CODEN: EKIDAT ISSN: 0374-3144
Language: German
Abstract: While active and **passive components** are readily produced for SMD, it is the components such as ICs, discrete semiconductors and **capacitors** which are the dominant components on the **circuit board** . Although these dominant components have gradually been adapted for SMD techniques, attempts to adapt switches and plugs have not been as successful since they are subject to mechanical stresses and loads. The mechanical and thermal stresses which switches and plugs must resist during surface **mounting** are detailed. Foil keys which satisfy the conditions for SMD could be a substitute for pressure keys (switches). Generally switches and plugs must be located in holes. Some manufacturers have made their switches suitable for SMD by making the housings washable. While DIP switches can readily be adapted to the SMD assembly tools, this is not the case with toggle switches.
Subfile: B

40/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

03051702 INSPEC Abstract Number: B88007135
Title: **Passive components** lead users into surface **mounting** terminations are crucial on the billions of chip **capacitors** and chip resistors used annually-and new standards will boost the use of resistor networks
Author(s): Pound, R.
Journal: Electronic Packaging and Production vol.27, no.6 p.59-60
Publication Date: June 1987 Country of Publication: USA
CODEN: ELPPA5 ISSN: 0013-4945
Language: English
Abstract: Chip **capacitors** and chip resistors are now the staple of surface-**mounting** activity. The consumption of surface-**mount** ICs and active discrete devices pales in comparison to the use of these surface-**mount passive components**. Chip **capacitors** and resistors, too, often are a user's first step into surface **mounting**-being placed on the bottom side of a printed **circuit board** and wave soldered.
Subfile: B

40/3,AB/9 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

01/06/2003

1880676 H.W. WILSON RECORD NUMBER: BAST99033121
SMT **passive components** save **circuit-board** space
AUGMENTED TITLE: models 3A425 and 3W525 from Anaren Microwave, Inc.
Browne, Jack;
Microwaves & RF v. 38 no5 (May 1999) p. 218
DOCUMENT TYPE: Product Evaluation ISSN: 0745-2993

ABSTRACT: A review of a series of surface-**mounted passive components** from Anaren Microwave, East Syracuse, New York, is presented. The devices, which have been named the Xingers, include baluns, hybrid couplers, directional couplers, and power dividers. The company asserts that the devices possess the performance of traditional RF/microwave **passive componentsand** are packaged to look like circuit elements such as **capacitors**.

40/3,AB/10 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15381489 PASCAL No.: 02-0069901
Lead zirconate titanate thin films on base-metal foils : An approach for embedded high-permittivity **passive components**
MARIA Jon-Paul; CHEEK Kevin; STREIFFER Stephen; KIM Seung-Hyun; DUNN Greg ; KINGON Angus
Department of Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina 27695, United States; Materials Science Division, Argonne National Laboratory, Argonne, Illinois 60439, United States; Motorola Advanced Technology Center, Schaumburg, Illinois 60196, United States
Journal: Journal of the American Ceramic Society, 2001, 84 (10) 2436-2438
Language: English
An approach for embedding high-permittivity dielectric thin films into glass epoxy laminate packages has been developed. Lead lanthanum zirconate titanate (Pb SUB 0 SUB . SUB 8 SUB 5 La SUB 0 SUB . SUB 1 SUB 5 -(Zr SUB 0 SUB . SUB 5 SUB 2 Ti SUB 0 SUB . SUB 4 SUB 8) SUB 0 SUB . SUB 9 SUB 6 O SUB 3 , PLZT) thin films were prepared using chemical solution deposition on nickel-coated copper foils that were 50 mu m thick. Sputter-deposited nickel top electrodes completed the all-base-metal **capacitor stack** . After high-temperature nitrogen-gas crystallization anneals, the PLZT composition showed no signs of reduction, whereas the base-metal foils remained flexible. The capacitance density was 300-400 nF/cm SUP 2 , and the loss tangent was 0.01-0.02 over a frequency range of 1-1000 kHz. These properties represent a potential improvement of 2-3 orders of magnitude over currently available embedded **capacitor** technologies for polymeric packages.

01/06/2003

28/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7362800 INSPEC Abstract Number: B2002-10-2120-004
Title: Reliability of thin-film resistors: impact of third harmonic screenings
Author(s): Kuehl, R.W.
Author Affiliation: BCcomponents BEYSCHLAG GmbH, Heide, Germany
Journal: Microelectronics Reliability vol.42, no.6 p.807-13
Publisher: Elsevier,
Publication Date: June 2002 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
SICI: 0026-2714(200206)42:6L.807:RTFR;1-9
Material Identity Number: G489-2002-005
U.S. Copyright Clearance Center Code: 0026-2714/02/$22.00
Language: English
Abstract: Third harmonic (TH) testing is a probably underrated in-line screen tool to detect and eliminate potential infant mortality failures in **passive components** that is not in the focus of current interest. The test is fairly rapid, convenient, and the associated equipment is relatively inexpensive. TH screening is thus advertised as a general means of ensuring robust behaviour of parts that pass this test. The author presents results of an evaluation of the present usage of this screen with a variety of thin-film resistors. A number of questions are considered, including: (1) how resistor manufacturers use this screen and how they establish accept/reject criteria, and the conclusions drawn from 20 years of experience with that method; (2) whether there are known physical and chemical defects that this screen misses; (3) whether rejected parts can be correlated with behaviour in short-term and long-term reliability tests; and (4) whether new, small, surface **mount** technology resistors can be reliably screened with TH testing and its limitations.
Subfile: B

28/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7150261 INSPEC Abstract Number: B2002-02-2130-014
Title: Electrical behavior of decoupling capacitors embedded in **multilayered** PCBs
Author(s): Madou, A.; Martens, L.
Author Affiliation: Dept. of Inf. Technol., Ghent Univ., Belgium
Journal: IEEE Transactions on Electromagnetic Compatibility vol.43, no.4 p.549-56
Publisher: IEEE,
Publication Date: Nov. 2001 Country of Publication: USA
CODEN: IEMCAE ISSN: 0018-9375
SICI: 0018-9375(200111)43:4L.549:EBDC;1-Q
Material Identity Number: I066-2002-001
U.S. Copyright Clearance Center Code: 0018-9375/01/$10.00
Language: English
Abstract: We describe the modeling of prototype capacitors embedded in **multilayered** printed circuit boards. We present the design of these devices. We also report measurement and characterization results. The emphasis is on the modeling of **via** hole connections to the embedded

capacitor, not on the technology of buried capacitors. Several designs have been compared with respect to their electrical behavior. In particular, several **via** hole configurations have been studied, because they are the main cause of parasitic behavior. With these buried capacitors, we obtained a reduction of the parasitic inductance of 80% compared to an equivalent discrete capacitor. This work has been carried out under a European Brite-EuRAM funded project COMPRISE (BE 96-3371). The objective of this project was to develop new materials and manufacturing processes to embed **passive components** (R, L, and C) within printed wiring structures fabricated from laminate materials. This technology enables the manufacture of space efficient and radio frequency (RF) optimal performing types of modules or board assemblies particularly suited to the market domain of portable and handheld communication and information technology products.
Subfile: B

28/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

7053154 INSPEC Abstract Number: B2001-11-6260C-034
Title: Design and characterization of 1.3/1.55 mu m optical transceiver using straight waveguide and double-filter photodiode
Author(s): Nakanishi, H.; Okada, T.; Shinkai, J.; Iguchi, Y.; Yamaguchi, A.; Yamabayashi, N.; Kuhara, Y.
Author Affiliation: Opto-Electron. R&D Labs., Sumitomo Electr. Ind. Ltd., Osaka, Japan
Journal: Transactions of the Institute of Electronics, Information and Communication Engineers C vol.J84-C, no.9 p.831-8
Publisher: Inst. Electron. Inf. & Commun. Eng,
Publication Date: Sept. 2001 Country of Publication: Japan
CODEN: DJTCEX ISSN: 1345-2827
SICI: 1345-2827(200109)J84C:9L.831:DC10;1-S
Material Identity Number: K840-2001-009
Language: Japanese
Abstract: A 1.3/1.55 mu m bi-directional transceiver has been successfully developed for ATM-PON system which is an international standard for optical access networks. Compact and low cost design was realized by introducing surface **mount** technology to integrate optical devices of an LD and a PD, active **electric devices** of ICs, and **passive components** of a WDM filter and an optical fiber. Reproducibility of SiO/sub 2/ waveguide was obtained by adopting a simple straight optical waveguide structure. A double-filter photodiode for a 1.55 mu m receiver has been newly developed in order to suppress optical crosstalk due to a 1.3 mu m transmitter LD. High optical output power of 0 dBm at 1.3 mu m and -40 dBm minimum receiver sensitivity at 155.52 Mbps have been obtained in a full duplex operation mode.
Subfile: B

28/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6946445 INSPEC Abstract Number: B2001-07-2120-005
Title: Electrical and stability properties and ultrasonic microscope characterisation of low temperature co-fired ceramics resistors
Author(s): Dziedzic, A.; Golonka, L.J.; Kita, J.; Thust, H.; Drue, K.-H.;

01/06/2003

Bauer, R.; Rebenklau, L.; Wolter, K.-J.
Author Affiliation: Inst. of Microsyst. Technol., Wroclaw Univ., Poland
Journal: Microelectronics Reliability vol.41, no.5 p.669-76
Publisher: Elsevier,
Publication Date: May 2001 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
SICI: 0026-2714(200105)41:5L.669:ESPU;1-I
Material Identity Number: G489-2001-005
U.S. Copyright Clearance Center Code: 0026-2714/2001/$20.00
Language: English
Abstract: This paper presents systematic investigations of electrical and stability properties of various low temperature co-fired ceramics (LTCC) resistors. One of the goals of this work was to check the compatibility of LTCC materials (tapes, **resistive** and **conductive** inks) from various manufacturers. Three commercially available green tapes and three LTCC resistor/conductor systems were examined. Resistive inks with 1 k Omega /sq. nominal sheet resistance were used. Buried and surface resistors were laminated and fired according to the tape manufacturers' recommendations. The influence of dimensional effects on sheet resistance and hot temperature coefficient of resistance, the temperature dependence of resistance in a wide temperature range (from -180 degrees C to +130 degrees C), long-term stability of thermally aged as-fired resistors (150 degrees C, 500 h) and durability to high-voltage micro- or nanosecond pulses (50 ns pulses with 4000 V/mm maximum electric field or 10 mu s ones with 700-1000 V/mm electrical field) were carried out for electrical and stability characterisation of LTCC resistors. Nondestructive scanning acoustic microscope diagnostics were applied for structure investigation and estimation of lamination and cofiring process quality of buried LTCC resistors.
Subfile: B

28/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6618642 INSPEC Abstract Number: B2000-07-2220J-003
Title: Next generation integral passives: materials, processes, and integration of resistors and capacitors on PWB substrates
Author(s): Bhattacharya, S.K.; Tummala, R.R.
Author Affiliation: Sch. of Electr. & Comput. Eng., Georgia Inst. of Technol., Atlanta, GA, USA
Journal: Journal of Materials Science: Materials in Electronics vol.11, no.3 p.253-68
Publisher: Kluwer Academic Publishers/Chapman & Hall,
Publication Date: April 2000 Country of Publication: USA
CODEN: JSMEEV ISSN: 0957-4522
SICI: 0957-4522(200004)11:3L.253:NGIP;1-2
Material Identity Number: H206-2000-005
U.S. Copyright Clearance Center Code: 0957-4522/2000/$15.00
Language: English
Abstract: The need for integral passives emerges from the increasing consumer demand for product miniaturization thus requiring components to be smaller and packaging to be space efficient. In this paper, the feasibility of integration of polymer/ceramic thin film (~5 mu m thick) capacitors (C) with other **passive components** such as resistors (R) and inductors (L) has been discussed. An integrated RC network requiring relatively large capacitance and resistance is selected as a model for co-integration of R and C components using low temperature PWB compatible fabrication processes. This test vehicle is a subset of a large

electrical circuit of a functional medical device. In order to produce higher capacitance density and reduce in-plane device area, **multi-layer** (currently two-layer) capacitors are **stacked** in the thickness direction. A commercially available Ohmega-Ply resistor/conductor material is selected for integral resistors. Resistors were fabricated using a multi-step lithography process with the utilization of two separate masks. Bottom copper electrodes for capacitors were also defined during the resistor fabrication process. Photodefinable epoxies filled with a high permittivity ceramic powder were used for fabrication of thin film capacitors. Epoxy and ceramic powders were mixed in the required proportion and blended using a high shear apparatus. The coating solution was homogenized in a roll miller for 3 to 5 days prior to casting in order to prevent settling of the higher density ceramic particles. Capacitors were fabricated by spin-coating on the sub-etched copper electrodes. The deposited dielectric layers were dried, exposed with UV radiation, patterned, and thermally cured. Top capacitor electrodes (copper) were deposited using a metal or an e-beam evaporator. The electrodes were patterned using the standard photolithography processes. Selected good samples were used for depositing the second capacitor layer. The RC network is extended to incorporate electroplated polymer/ferrite core micro-inductors through the fabrication of an industry prototype low pass RLC filter. Meniscus coating was evaluated for large area manufacturing with high process yield. A capacitance density of ~3 nF cm/sup -2/ was obtained on a single layer capacitor with ~6 mu m thick films. The capacitance density was increased to ~6 nF cm/sup -2/ with the two-layer deposition process. The capacitors were relatively stable up to a frequency range of 120 Hz to 100 kHz. Meniscus coating was qualified to be a viable manufacturable method for depositing polymer/ceramic capacitors on large area (300 mm*300 mm) PWB substrates. Dielectric constant values in the range of 3.5 to 35 with increase in filler loading up to 45 vol% were achieved in the epoxy nanocomposite system where the dielectric constant of the host polymer was limited to ~3.5. Higher dielectric constant polymers are required to meet the increasingly higher capacitance needs for the next generation electronics packaging. Possible avenues for achieving higher capacitance density in polymer/ceramic nanocomposite system have been discussed.

Subfile: B

28/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

6614837 INSPEC Abstract Number: B2000-07-0170J-050

Title: Properties of joints realized by electrically conductive adhesives

Author(s): Mach, P.; Skvor, M.

Author Affiliation: Dept. of Electrotechnol., Czech Tech. Univ., Prague, Czech Republic

Conference Title: 12th European Microelectronics and Packaging Conference. Proceedings p.284-9

Publisher: Int. Microelectron. & Packaging Soc.-Europe, Cambridge, UK

Publication Date: 1999 Country of Publication: UK xlii+606 pp.

ISBN: 0 9535858 0 8 Material Identity Number: XX-1999-02235

Conference Title: Proceedings of IMAPS-EUROPE '99. 12th European Microelectronics and Packaging Conference

Conference Date: 7-9 June 1999 Conference Location: Harrogate, UK

Language: English

Abstract: The resistance and current vs. voltage characteristics nonlinearity of joints manufactured using electrically conductive adhesives (ECA) were investigated. These measurements were completed with a limited

number of noise measurements. The joints were manufactured using six different types of adhesive by assembly of resistors with "zero" resistance (their measured resistance was 5 m Omega) on **FR4** boards. The surface finish on the boards was either copper or gold-plated copper. The resistors were of type 1206, recommended for assembly using ECA. Their nonlinearity and noise were very low in comparison with the nonlinearity and noise of the joints. The measurements were performed using four-point connection of the resistors. The specimens were thermally aged at a temperature of 160 degrees C. It was found that the resistance and nonlinearity of the joints increased after thermal aging and that this increase depends on the aging time. A longer aging time caused greater increase of the investigated parameters. The aim of the work was to analyze in particular the nonlinearity of the joints as a new parameter for evaluation of their properties and therefore measurements of the noise voltage were performed for a limited number of joints only. It was found that the changes in noise voltage are similar to the changes in nonlinearity.
Subfile: B

28/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

6383862 INSPEC Abstract Number: B1999-12-2130-001
Title: Development of ultra-low fire COG and X7R dielectric compositions for **multilayer** ceramic chip capacitor and integrated **passive component** applications
Author(s): Foster, B.C.; Symes, W.J.
Author Affiliation: Transelco Div., Ferro Corp., Penn Yan, NY, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3582 p.246-51
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3582L.246:DUFD;1-K
Material Identity Number: C574-1999-173
Conference Title: 1998 International Symposium on Microelectronics
Conference Sponsor: SPIE; IMAPS
Conference Date: 1-4 Nov. 1998 Conference Location: San Diego, CA, USA
Language: English
Abstract: A series of COG and X7R dielectric compositions have been developed which densify at temperatures below 1000 degrees C. These compositions have been demonstrated to be compatible with 90:10 and 95:5 AgPd internal electrode metal systems in **multilayer** ceramic capacitor devices. In addition, these devices have been subjected to mechanical, electrical and environmental reliability testing and have exhibited failure rates that meet accepted industry standard pass/fail criteria. A feasibility study in which multiple dielectric constant materials were co-fired in a monolithic structure indicates that these materials are good candidates for integrated **passive component** applications. A **multilayer** ceramic capacitor cost model shows that when these materials are used with 95:5 AgPd, the total material cost independent of processing cost is lower than the material cost for Ni electrode material systems.
Subfile: B

28/3,AB/8 (Item 8 from file: 2)

01/06/2003

DIALOG(R)File 2:INSPEC

6258390 INSPEC Abstract Number: B1999-07-0170Q-003
Title: Reduction of lead-content in lead-wire-coatings, technical impacts and application-experiences
Author(s): Burstner, G.; Frohlich, E.
Author Affiliation: Feindrahtwerk Adolf Edelhoff GmbH & Co., Iserlohn, Germany
Conference Title: 18th Capacitor and Resistor Technology Symposium. CARTS '98 p.235-41
Publisher: Components Technol. Inst, Huntsville, AL, USA
Publication Date: 1998 Country of Publication: USA 266 pp.
Material Identity Number: XX-1997-01940
Conference Title: Proceedings of CARTS-USA 96
Conference Sponsor: Components Technol. Inst.; IEEE; Int. Microelectron. & Packaging Soc
Conference Date: 9-13 March 1998 Conference Location: Huntington Beach, CA, USA
Language: English
Abstract: The reduction of Pb-content has become a major topic for the design and production of **passive components**, whether they are leaded or SMDs. Multinational companies started to create safety regulations where end-products which contain lead must be registered and accepted by special procedures. Other companies announced the use of totally Pb-free alloys in production. The tendency to avoid Pb use entirely is therefore set to increase. In this paper, specific attention is given to: various coating technologies; single layer and **multilayer** coatings; impact of Pb reduction and Sn enrichment; impact on **passive component** production processes. Recommendations are given with regard to coating technology, production parameters, and step-wise Pb reduction. This information is intended to support **passive component** producers who have to change their present product specification, and/or their existing production process. Milestones for producing a Pb-reduced or even Pb-free component can be found.
Subfile: B

28/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

6250841 INSPEC Abstract Number: B1999-06-2140-008
Title: Evaluation of advanced `wet-stack' materials in a test planar inductor design
Author(s): Murray, C.; O'Donnell, T.; O'Reilly, S.; Flannery, J.; Collins, D.; O Mathuna, S.C.
Author Affiliation: Nat. Microelectron. Res. Centre, Univ. Coll. Cork, Ireland
Conference Title: 17th Capacitor and Resistor Technology Symposium. CARTS '97 p.47-55
Publisher: Components Technol. Inst, Huntsville, AL, USA
Publication Date: 1997 Country of Publication: USA 326 pp.
Material Identity Number: XX-1997-01941
Conference Title: Proceedings of CARTS USA 1997
Conference Sponsor: Components Technol. Inst.; IEEE; Int. Microelectron. & Packaging Soc
Conference Date: 24-27 March 1997 Conference Location: Jupiter, FL, USA
Language: English

Abstract: Co-fired wet stack processing offers a route towards the realisation of high performance **multilayer passive components** . Chip inductors, inductor arrays and transformers for low profile SMPS in portable applications can all be fabricated by this method. This paper evaluates the performance of wet stack ferrite and silver conductor materials which have recently become commercially available. A two layer, six turn test inductor was fabricated by means of wet stack processing and electrically characterised. Using three different ferrite materials of quoted permeability mu =16, 60 and 171 in this device, inductances were measured to be L/sub s/=0.63 mu H, 1.43 mu H and 4.38 mu H, respectively. Peak Q values ranged from 22 to 47, which are superior to similar thick film ferrite and air-core parts which were also fabricated and tested. Measured electrical and magnetic characteristics were employed in analytical and finite element models of the inductors in an effort to achieve a predictive design capability.
Subfile: B

28/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

6250840 INSPEC Abstract Number: B1999-06-2130-030
Title: Material science issues in electroceramic components: a university perspective
Author(s): Randall, C.A.; Cann, D.P.; McCauley, D.; Toal, F.J.; Hitomi, A.; Hackenberger, W.; Shrout, T.R.
Author Affiliation: Mater. Res. Lab., Pennsylvania State Univ., University Park, PA, USA
Conference Title: 17th Capacitor and Resistor Technology Symposium. CARTS '97 p.28-34
Publisher: Components Technol. Inst, Huntsville, AL, USA
Publication Date: 1997 Country of Publication: USA 326 pp.
Material Identity Number: XX-1997-01941
Conference Title: Proceedings of CARTS USA 1997
Conference Sponsor: Components Technol. Inst.; IEEE; Int. Microelectron. & Packaging Soc
Conference Date: 24-27 March 1997 Conference Location: Jupiter, FL, USA
Language: English
Abstract: Technological advancements in semiconductor fabrication have forced **passive components** to continually undergo miniaturization while requiring new methods of component packaging. The evolution of surface **mount** technology (SMT) has led to **multilayer** capacitors (MLCs) with dielectric thickness approaching 1 mu m in 0402 sized components. Fundamental issues regarding scale arise, including dielectric cooperative phenomena, controlling defect chemistry and degradation rates, and the effects of electrode interfacial chemistry, all of which may affect device performance. Furthermore, the cost of component placement is projected at more than 300% of the individual component itself. Clearly, the trend in SMT requires the integration of **passive components**. In addition to scale, integration, both in discrete-like and integrated packages, brings about a number of processing issues, including the ability to cofire electroceramics. In this work, we touch upon a few of the scientific issues to demonstrate how universities can play a role in aiding materials suppliers and component manufacturers. These include: grain and crystallite size effects, defect chemistry and role of degradation limiting additives in base metal electrode MLCs, defect formation at the electrode-ceramic interface and the co-sintering of different materials.

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28/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

6238999 INSPEC Abstract Number: B1999-06-0170N-008
Title: An example of failure analysis on high-reliable electronic components (capacitors, resistors, and filters)
Author(s): Fujimoto, N.
Author Affiliation: Dept. of Quality Assurance, Mitsubishi Electr. Corp., Kamakura, Japan
Conference Title: 16th Capacitor and Resistor Technology Symposium. CARTS '96 p.86-90
Publisher: Components Technol. Inst, Huntsville, AL, USA
Publication Date: 1996 Country of Publication: USA 320 pp.
Material Identity Number: XX-1996-00209
Conference Title: Proceedings of 16th Capacitor and Resistor Technology Symposium
Conference Sponsor: Components Technol. Inst.; IEEE; Microelecton. Soc
Conference Date: 11-15 March 1996 Conference Location: New Orleans, LA, USA
Language: English
Abstract: The role of reliability grows more important in the development of electronic equipment for diverse applications, since the equipment has become more sophisticated while being increasingly downsized at the same time. In order to meet such requirements as high reliability, small size, and multifunctionality, both high reliability components and established surface **mount** technology are needed. The evaluation of the components through destructive physical analysis as well as the analysis of printed circuit assemblies (PCAs) with surface **mount** devices (SMDs) are performed. This evaluation allows the purchase of high reliability components, thus improving product reliability in the Mitsubishi Electric Corporation Kamakura Works (MELCO). Examples of integrated quality improvement activities on **passive components** such as capacitors, resistors and EMI filters are reported here, which are the result of consolidated efforts by component manufacturers and the systems side at MELCO.
Subfile: B

28/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

6232488 INSPEC Abstract Number: B1999-06-2340E-019
Title: Thermionic vacuum integrated microcircuits as mechanical transducers
Author(s): Mukhurov, N.I.
Author Affiliation: Inst. of Electron., Acad. of Sci., Byelorussia
Conference Title: Eleventh International Vacuum Microelectronics Conference. IVMC'98 (Cat. No.98TH8382) p.160-1
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xxv+358 pp.
ISBN: 0 7803 5096 0 Material Identity Number: XX-1998-02841
Conference Title: Eleventh International Vacuum Microelectronics Conference. IVMC'98
Conference Sponsor: IEEE

Conference Date: 19-24 July 1998 Conference Location: Asheville, NC, USA
Language: English
Abstract: Dielectric layers of anodic alumina (AA) are widely used as substrates and insulating elements in various design configurations of **electron devices**. Combination of anodizing with photolithographic and etching processes as well as vacuum deposition of **conductive, resistive,** semiconductor and dielectric films makes it possible to create, in a three-dimensional dielectric structure, holes, cavities, etc., with thin-film microcircuit components formed to a high degree of accuracy on different levels (with respect to the main working surface of the substrate). Three-dimensional multilevel microreliefed substrates form a structural basis of unique thermo- and radiation-resistant thermionic VIMCs. The possibility has been demonstrated of making simple logic and analog **electrical circuits** in the form of VIMC. Particular promising is the use of porous anodic alumina substrates for fabrication of multi-point field emitters where the size of each cell lies within several thousand angstrom.
Subfile: B

28/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

6186599 INSPEC Abstract Number: B1999-04-2120-003
Title: Study of correlation among differential nonlinearity, nonlinearity and noise of thick film resistors
Author(s): Mach, P.J.; Svasta, P.M.
Author Affiliation: Czech Tech. Univ., Prague, Czechoslovakia
Journal: Informacije MIDEM vol.28, no.3 p.149-53
Publisher: Soc. Microelectron. Electron. Components & Mater.-MIDEM,
Publication Date: Sept. 1998 Country of Publication: Slovenia
CODEN: IMIDEN ISSN: 0352-9045
SICI: 0352-9045(199809)28:3L.149:SCAD;1-H
Material Identity Number: N527-1999-001
Language: English
Abstract: Typical parameters which make the reliability assessment of thick film resistors possible are noise and the nonlinearity of a current vs. voltage characteristic. Both of these parameters are strongly influenced by mechanisms of film conductivity and by mechanisms of conductivity which appear inside a transient area between the resistive film and its conductive contact. A study of correlation between the nonlinearity, differential nonlinearity and noise of thick film resistors was carried out. The influence of the form and trimming of the resistors on these parameters was investigated. It was found that the form of the resistors influences both of these parameters similarly. Trimming of the resistors influences the noise substantially, but its influence on the nonlinearity is very low.
Subfile: B

28/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

6015880 INSPEC Abstract Number: B9810-0170Q-002
Title: Environmental evaluation of **passive components** with life cycle assessment

01/06/2003

Author(s): Van der Wel, H.; Reijnen, F.J.
Author Affiliation: Philips Centre for Manuf. Technol., Eindhoven, Netherlands
Conference Title: 11th European Passive Components Symposium CARTS-EUROPE '97 Proceedings p.147-51
Publisher: Electron. Components Inst. Int, Crowborough, UK
Publication Date: 1997 Country of Publication: UK xi+180 pp.
Material Identity Number: XX97-01939
Conference Title: Proceedings of CARTS-EUROPE 11th Annual European Passive Components Conference
Conference Sponsor: Electron. Components Inst. Int.; Int. Microelectron. & Packaging Soc
Conference Date: 14-16 Oct. 1997 Conference Location: Prague, Czech Republic
Language: English
Abstract: Process inventories and environmental evaluations with the life cycle assessment (LCA) method were made for the production of ceramic **multilayer** capacitors, surface **mounted** device (SMD) and conventional resistors. In this paper, the LCA method and its results for products of Philips **Passive Components** are discussed.
Subfile: B

28/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

5678008 INSPEC Abstract Number: B9710-2140-002
Title: A planar inductor fabricated using co-fired wet stack ferrite processing
Author(s): Murray, C.; Flannery, J.; Mathuna, S.C.O.
Author Affiliation: Nat. Microelectron. Res. Centre, Univ. Coll. Cork, Ireland
Conference Title: 10th European Passive Components Symposium. CARTS-EUROPE '96 p.215-20
Publisher: Electron. Components Inst. Int, Crowborough, UK
Publication Date: 1996 Country of Publication: UK xii+264 pp.
Material Identity Number: XX96-02667
Conference Title: Proceedings of CARTS-EUROPE '96
Conference Sponsor: Electron. Components Inst. Int.; ISHM-Microelectron. Soc
Conference Date: 7-11 Oct. 1996 Conference Location: Nice, France
Language: English
Abstract: Co-fired wet stack processing offers a route towards the realisation of high performance **multilayer passive components** such as inductors, transformers and filters. A two layer, six turn planar magnetic test inductor was fabricated by means of wet stack processing using newly available ferrite and silver conductor materials. Inductance, resistance, Q factor and self resonant frequency (SRF) were measured for devices containing ferrite of permeability mu =16. Typical inductances of 0.6 mu H with a Q value of 36 at 10 MHz were and SRF of 48 MHz were measured for fabricated parts. This is superior to a similar experimental thick-film ferrite device with L=0.9 mu H, Q=6 and SRF=39 MHz. Models of the devices were developed using finite element analysis. Accurate materials characterisation was essential for accurate models. Simulations were correlated with previously published work to provide a route towards a predictive design capability for planar magnetic device fabrication.
Subfile: B

01/06/2003

28/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

5592878 INSPEC Abstract Number: B9707-2140-007
Title: High-quality RF inductors in LTCC
Author(s): Muller, J.
Author Affiliation: Dept. of Electr. Eng., Tech. Univ. Ilmenau, Germany
Journal: Microelectronics International no.43 p.59-63
Publisher: Wela Publications,
Publication Date: May 1997 Country of Publication: UK
CODEN: MIINF2 ISSN: 1356-5362
SICI: 1356-5362(199705)43L.59:HQIL;1-R
Material Identity Number: D084-97002
Language: English
Abstract: Low temperature cofired ceramics (LTCCs) combine the advantages of both **multilayer** substrates with excellent high-frequency properties and a high-conductivity metallisation. The possibility of realising **passive components** embedded in the glass ceramics increases the scale of integration. Inductors are designed as single-layer (planar spiral) or **multilayer** (3D) arrangements of narrow conductive traces with useful values up to a few hundred nanohenry. This range makes them useful for high-frequency applications. Although the conductor pastes used have a low resistance, the maximum quality factor of these coils seldom exceeds 60. The decisive parameter in this regard is the line thickness which is normally 10-15 mu m. A novel technique based on laser scribed canals permits conductor patterns with an almost square cross-section, thus reducing the line resistance by a factor up to 10. Coils manufactured by this method have a considerably improved quality and are able to withstand high currents. This property widens the range of applications for LTCCs into the field of high-power electronics.
Subfile: B

28/3,AB/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

5391147 INSPEC Abstract Number: B9611-0100-032
Title: Proceedings of First Pan Pacific Microelectronics Symposium
Publisher: Surface Mount Technol. Assoc, Edina, MA, USA
Publication Date: 1996 Country of Publication: USA 312 pp.
Material Identity Number: XX95-03167
Conference Title: Proceedings of First Pan Pacific Microelectronics Symposium
Conference Date: 6-8 Feb. 1996 Conference Location: Honolulu, HI, USA
Language: English
Abstract: The following topics were dealt with: world markets; advanced single chip packaging; high density interconnection technology; direct chip attach; high performance wiring boards; suface **mount** reliability; passive/reactive component technologies; area array; business management.
Subfile: B

28/3,AB/18 (Item 18 from file: 2)
DIALOG(R)File 2:INSPEC

01/06/2003

5382383 INSPEC Abstract Number: B9611-2120-003
Title: One percent resistors-but are they?
Author(s): Yarnall, R.
Journal: Electronic Product Design vol.17, no.8 p.27, 30
Publisher: IML Techpress,
Publication Date: Aug. 1996 Country of Publication: UK
CODEN: EPDEDB ISSN: 0263-1474
SICI: 0263-1474(199608)17:8L.27:PRT;1-Q
Material Identity Number: E302-96008
Language: English
Abstract: With the move from leaded components to surface **mount**, many resistor users have made the switch-some unwittingly-from metal film technology to thick film technology. The most commonly-available type of resistor today is the thick film chip 1206 or 0805. This switch in technology, together with the better heat transfer inherent in surface **mount** components, gives rise to the possibility of large shifts in resistance value. Whilst thick film resistors are considerably cheaper than metal film, it is frequently not realised that a thick film resistor that is within 1% on delivery may be adrift by as much as 3.5% once **mounted** on the board, and up to 9% out after 8,000 hours service. All of these shifts may be within the components' specifications; the distinction to be noted is between initial tolerance and various measures of stability.
Subfile: B

28/3,AB/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC

5237799 INSPEC Abstract Number: B9605-2250-029
Title: Thin film integral capacitor fabricated on a polymer dielectric for high density interconnect (HDI) applications
Author(s): Paik, K.W.; Toh-Ming Lu
Author Affiliation: Dept. of Mater. Sci. & Eng., Korea Adv. Inst. of Sci. & Technol., Taejon, South Korea
Conference Title: Electronic Packaging Materials Science VIII. Symposium p.33-8
Editor(s): Sundahl, R.C.; Tu, K.-T.; Jackson, K.A.; Borgesen, P.
Publisher: Mater Res. Soc, Pittsburgh, PA, USA
Publication Date: 1995 Country of Publication: USA xi+284 pp.
Material Identity Number: XX96-00317
Conference Title: Electronic Packaging Materials Science VIII. Symposium
Conference Date: 17-20 April 1995 Conference Location: San Francisco, CA, USA
Language: English
Abstract: The expanding needs of mixed signal applications of thin film MCM technologies which combine analog, digital, power and opto-**electric devices** require a wide range of integral thin film **passive components** within the MCM structure. There is a need to incorporate these passive elements into the interconnect structure to reduce component count, decrease substrate area and improve electrical performance. In this study, we investigated advanced materials and processing technologies for in situ formation of capacitor components during fabrication of **multilayer** polymer/copper interconnect structures. An amorphous BaTiO/sub 3/ film with a dielectric constant of 10 to 40, depending on stoichiometry, was deposited on a surface roughness controlled metallized polyimide surface at room temperature using the reactive partial ionized beam (RPIB) technique. Simple

metal/insulator/metal (MIM) capacitors were fabricated and characterized. Hundreds of pF capacitance with <10/sup -6/ A leakage current were obtained depending on the top metal electrode size, dielectric thickness, and dielectric film stoichiometry. Annealing the dielectric film significantly enhanced the leakage current property. After thermal cycling treatment, it was proved that the thin film integral capacitor was reliable enough to be used in practical MCM applications. Process defect control was necessary to improve capacitor yield.
Subfile: B

28/3,AB/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC

04265142 INSPEC Abstract Number: B9212-0100-015
Title: 5th European Capacitor and Resistor Technology Symposium CARTS - Europe '91
Publisher: Electron. Components Inst. Int, Crowborough, UK
Publication Date: 1991 Country of Publication: UK xi+276 pp.
Conference Sponsor: Electron. Components Inst. Int
Conference Date: 30 Sept.-3 Oct. 1991 Conference Location: Munich, Germany
Language: English
Abstract: The following topics were dealt with: component standardisation; materials and terminations; applications; technology and processing; **passive components** market; surface **mount** and ceramic technology; quality assurance and reliability; products description and capabilities; and failure analysis.
Subfile: B

28/3,AB/21 (Item 21 from file: 2)
DIALOG(R)File 2:INSPEC

03820506 INSPEC Abstract Number: B91008687, C91014949
Title: Practical implementation of SPC in a manufacturing workshop
Author(s): Gainvet, C.
Author Affiliation: LCC, Seurre, France
Conference Title: 4th European Capacitor and Resistor Technology Symposium. CARTS - EUROPE '90 p.157-62
Publisher: ECII, Crowborough, UK
Publication Date: 1990 Country of Publication: UK xiv+280 pp.
Conference Sponsor: Electron. Components Inst. Int
Conference Date: 8-11 Oct. 1990 Conference Location: Bordeaux, France
Language: English
Abstract: Thomson-LCC Company is a **passive components** manufacturer. The Seurre factory produces more than three million **stacked** polyester film capacitors, with 5 mm pitch, per day. Workshop is divided in 12 manufacturing steps, with about 100 machines and 200 persons working. After one year, 15 key parameters are monitored with SPC. Main results are: yield 2.4% up on 1988; final ppm level 40% down on 1988; overall scraps cost 30% lower than in 1988; and no controller left in QA department (all controls integrated in production lines).
Subfile: B C

28/3,AB/22 (Item 22 from file: 2)
DIALOG(R)File 2:INSPEC

01/06/2003

03330949 INSPEC Abstract Number: B89026291
Title: Testing resistors, coils and capacitors rapidly and precisely
Author(s): Gosselink, M.
Journal: Elektronik vol.37, no.26 p.81
Publication Date: 23 Dec. 1988 Country of Publication: West Germany
CODEN: EKRKAR ISSN: 0013-5658
Language: German
Abstract: The author briefly describes Rood Testhouse's automatic impedance analysis station intended to eliminate human error in the testing of **passive components**. The station consists of a HF impedance analyser (HP4191A) for 1-100 MHz, a LF impedance analyser (HP4192A) for up to 1 GHz, and a universal tester (HP4328A)-all three connected **via** an IEEE bus to a computer (HP9816). The author outlines the advantages and the savings in time, explaining selected procedures such as coil testing and measurement display and recording.
Subfile: B

28/3,AB/23 (Item 23 from file: 2)
DIALOG(R)File 2:INSPEC

01584322 INSPEC Abstract Number: B80048871
Title: Picominiaturized **passive components**
Author(s): Avery, G.E.
Journal: Military Electronics/Countermeasures vol.6, no.3 p.52-5
Publication Date: March 1980 Country of Publication: USA
CODEN: MELCDM ISSN: 0164-4076
Language: English
Abstract: Describes batch fabrication processes used to produce monolithic microchip **passive components** for applications in the 20 MHz to 6 GHz frequency range. L, R and C planar components and structures combining all three are produced by a **multilayer** thin film process using vacuum deposition techniques.
Subfile: B

28/3,AB/24 (Item 24 from file: 2)
DIALOG(R)File 2:INSPEC

00551019 INSPEC Abstract Number: A73059239
Title: Catalogue of right ascensions of 645 FKSZ stars in the **FR4** system
Author(s): Vagushchenko, L.L.
Journal: Astrometriya i Astrofizika no.16 p.3-12
Publication Date: 1972 Country of Publication: Ukrainian SSR, USSR
CODEN: AAFZBZ ISSN: 0582-8198
Language: English
Abstract: Observations of right ascensions of 645 FKSZ stars were conducted with the meridian circle of the Odessa Observatory. A catalogue has been compiled and compared with some other catalogues. The mean square error of a single observation is +or-0.024. An **electromagnetic device** for driving the right ascension screw was used.
Subfile: A

28/3,AB/25 (Item 25 from file: 2)
DIALOG(R)File 2:INSPEC

01/06/2003

00534460 INSPEC Abstract Number: B73025745
Title: 23rd Electronic Components Conference
Publisher: IEEE, New York, NY, USA
Publication Date: 1973 Country of Publication: USA vii+363 pp.
Conference Sponsor: IEEE; Electronic Industries Assoc
Conference Date: 14-16 May 1973 Conference Location: Washington, DC, USA
Language: English
Abstract: The following topics were dealt with: emerging component technologies; interconnections; laser trimming techniques; manufacturing techniques; **passive components**; thick film materials; **multilayer** hybrids; thin film materials; and thermal effects and reliability.
Subfile: B

28/3,AB/26 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1607644 NTIS Accession Number: TIB/A91-01279
Schaltungsentwicklung fuer hochbitratige optoelektronische Uebertragungss ysteme. Abschlussbericht. (Circuit development for high bit rate optoelectronic transmission systems. Final report)
Rosenzweig, J. ; Axmann, A. ; Benz, W. ; Berroth, M. ; Bosch, R.
Fraunhofer-Inst. fuer Angewandte Festkoerperphysik, Freiburg im Breisgau (Germany, F.R.).
Corp. Source Codes: 102007000; 2567200
Apr 91 71p
Languages: German
Journal Announcement: GRAI9124
In German.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC E09
The aim of the research was to design, manufacture and test optoelectronic transmission systems operating at 10 Gbit s (-1) . A manufacturing technology based on GaAs/AlGaAs heterostructure field-effect transistors was developed at the Fraunhofer Institute of Applied Solid State Physics (IAF). This technology included the production of metal semiconductor metal (MSM) photodiodes, HFETs, NiCr resistors, capacitances, inductances, coplanar lines and air bridges. All active and **passive components** have been characterised electrically at dc and ac (using s parameters and optical correlation measurements). The active components i.e. the transistors and the photodetectors, have been simulated by means of the Monte Carlo particle model. The computer aided design manual and a SPICE based circuit simulator needed to design the circuits have also been developed. A system concept for communication **via** 850 nm wavelength light was agreed with Siemens. Siemens concentrated their effort on the transmitter which consisted of a laser diode and driver, IAF developed the receiver photodiode with its transimpedance amplifier, clock recovery, bit synchroniser and a 1:4 demultiplexer. The integrated photodiode and preamplifier functioned at a bit rate of 10 Gbit s (-1) . The ability to function at this rate was also proven for the bit synchroniser (the frequency divider worked up to 14.2 GHz) and the 1:4 demultiplexer up to 11.6 Gbit s (-1) . An optical transmission system for light of wavelength 1550 nm was developed in collaboration with SEL. SEL designed the necessary

circuits which were manufactured at IAF. The wafers handed over to SEL contained several capable laser drivers and pre- and mainamplifiers. (orig.). (Available from TIB Hannover: FR 5059+a.) (Copyright (c) 1991 by FIZ. Citation no. 91:001279.)

28/3,AB/27 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

1601395 NTIS Accession Number: N91-27476/1
60 GHz Solid State Power Amplifier
(Final Report)
Mcclymonds, J.
Raytheon Co., Lexington, MA.
Corp. Source Codes: 006831000; RI851220
Sponsor: National Aeronautics and Space Administration, Washington, DC.
Report No.: NAS 1.26:188669; NASA-CR-188669
1 Mar 91 62p
Languages: English
Journal Announcement: GRAI9122; STAR2919
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A04/MF A01
A new amplifier architecture was developed during this contract that is superior to any other solid state approach. The amplifier produced 6 watts with 4 percent efficiency over a 2 GHz band at 61.5 GHz. The unit was 7 x 9 x 3 inches in size, 5.5 pounds in weight, and the conduction cooling through the baseplate is suitable for use in space. The amplifier used high efficiency GaAs IMPATT diodes which were **mounted** in 1-diode circuits, called modules. Eighteen modules were used in the design, and power combining was accomplished with a proprietary **passive component** called a combiner plate.

28/3,AB/28 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01678661 AAD9912103
ACCURATE AND EFFICIENT INTEGRAL EQUATION MODELING OF THREE-DIMENSIONAL, PASSIVE HIGH-FREQUENCY CIRCUIT COMPONENTS (**PASSIVE COMPONENTS**, PORTABLE ELECTRONICS)
Author: HECKMANN, DAVID L.
Degree: PH.D.
Year: 1998
Corporate Source/Institution: THE UNIVERSITY OF ARIZONA (0009)
Source: VOLUME 59/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 5990. 121 PAGES

Recent advances in **multi-layer** insulating substrates, such as low temperature co-fired ceramic (LTCC), have motivated novel designs of RF/microwave **passive components**, such as filters, couplers and power combiners, which attempt to take advantage of the third dimension in order to reduce component size. Such designs are highly desirable for miniature transceiver realizations in portable **electronic devices**. In addition to advances in new materials and manufacturing processes, an important enabling technology for the realization of such systems is a three-dimensional electromagnetic modeling tool capable of

providing the accuracy and computational efficiency necessary for design iteration in a three-dimensional conductor layout.

We present a novel approach to the frequency-domain integral-equation modeling of conducting structures embedded in a homogeneous dielectric that is shielded by two perfectly-conducting ground planes. Novel closed-form expressions for the impedance matrix elements arising from a Method of Moments solution of the integral equation are developed. These exact expressions were found to improve the computational efficiency over direct numerical integration by two orders of magnitude, greatly reducing matrix fill times. Several simple structures, including a transmission line and three microwave filters are simulated to test and validate the developed expressions.

28/3,AB/29 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01410767 AADAAIC409205
THE OHMIC CONTACT FORMATION IN NICKEL/GOLD/TELLURIUM/GOLD/GALLIUM ARSENIDE AND GERMANIUM/PALLADIUM/GALLIUM ARSENIDE STRUCTURES
Author: WATTE, JAN
Degree: PH.D.
Year: 1994
Corporate Source/Institution: KATHOLIEKE UNIVERSITEIT LEUVEN (BELGIUM) (5605)
Source: VOLUME 56/02-C OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 490. 143 PAGES
Location of Reference Copy: K. U. LEUVEN, EXACTE WETENSCHAPPEN, CAMPUSBIBLIOTHEEKDIENST, CELESTIJNENLAAN 300 A, B-3001 LEUVEN (HEVERLEE), BELGIUM

Metal/semiconductor contacts play a vital role in micro-**electronic circuits** since they provide the communication of the interior of a device with the outside world. One distinguishes Schottky barrier contacts (rectifying) and ohmic contacts (with a linear current-voltage characteristic and a resistivity negligibly small compared to the resistivity of the bulk). The objective of this work was to correlate by a combined Raman and X-ray diffraction analysis doping effects, defect and phase formation at the GaAs interface in Ni/Au/Te/Au/n-GaAs and Ge/Pd/n-GaAs structures with the electrical modifications of these structures after furnace and laser beam mixing.

The conclusion that could be drawn from our characterization study is that Ni provides a more uniform formation of $\rm Ga\sb2Te\sb3$ crystallites at the GaAs interface compared to Au/Te/Au/GaAs contacts. No excessive doping of the GaAs to players could be found. The ohmic properties can be explained in terms of the formation of a $\rm n\sp+$-$\rm Ga\sb2Te\sb3/GaAs$ heterojunction. Ohmic contacts obtained after laser beam mixing were also investigated. For these structures low **resistive conductivity** can be obtained in two intermixing regimes. Irradiation with low energy density and multiple pulses promotes the formation of a $\rm Ga\sb2Te\sb3/GaAs$ heterojunction whereas irradiation with high energy densities gives rise to the formation of an amorphous/highly defective heterojunction.

In furnace annealed Ge/Pd/GaAs ohmic contacts the GaAs interface is atomically abrupt. Backside Raman measurements revealed that a quasi two dimensional excessive doping is created in the GaAs toplayers. In addition, a thin Ge layer grown epitaxially on the $\rm n\sp+$-GaAs layer, plays a non negligible role in providing low **resistive conductivity**.

01/06/2003

28/3,AB/30 (Item 1 from file: 89)
DIALOG(R)File 89:GeoRef

02328709 GEOREF NO.: 99-065773
TITLE: Modelling an ultra-long **electrical device**, and application in interpretation of a hot dry rock geothermal reservoir
AUTHOR(S): Lovell, John; Miyairi, Makoto; Tezuka, Kazuhiko; Mowat, Gordon
CORPORATE SOURCE: Schlumberger-Doll Research, Ridgefield, CT, United States
CORPORATE SOURCE: ; Japex Research Centre
MONOGRAPH TITLE: Proceedings of the Nineteenth annual convention; Volume 2, Engineering
AUTHOR(S): Tweed, J. L.
CORPORATE SOURCE: Indonesian Petroleum Association Lecture Committee, Indonesia
CONFERENCE TITLE: Nineteenth annual convention, Indonesian Petroleum Association
CONFERENCE LOCATION: Jakarta, Indonesia,
CONFERENCE DATE: Oct. 16-18, 1990
PUBLISHER: Indonesian Petroleum Association, Jakarta, Indonesia
SOURCE: Proceedings of the Annual Convention - Indonesian Petroleum Association vol. 19, Vol. 2 p. 457-477
DATE: 1990
ISSN: 0126-1126
LANGUAGE: English
ABSTRACT: Various arrays of pole-pole and dipole-dipole electrical logs of standard up to ultra-long spacings have been modelled in an environment of **conductive** borehole and **resistive** formation. The forward modelling has been done with a 2D finite element code solving Laplace's Equation. As the frequency of the measure currents is sufficiently low, the skin depth is much larger than the distances involved, and therefore the additional complication of a full Helmholtz Equation solution is unnecessary. The code has been run on various synthetic conductivity models in order to determine the effects of **resistive** and **conductive** shoulder beds, of conductive invasion, and of the conductive borehole. Logs of the same electrode configurations and spacings have been run in a well drilled in a hot dry rock (HDR) geothermal reservoir in Hijiori, Honshu, Japan. The existence of both local mechanical-and thermal-stress-related fractures close to the borehole as well as natural fractures intersecting the borehole has been confirmed by sonic, natural gamma, flowmeter, and temperature logs. This fracturing requires the introduction of a conductive invaded zone. The electrical logs have been inverted by iterative forward modelling using the same 2D finite element code in order to derive a model of rock conductivity which is horizontally layered, invaded by wellbore fluid, and incorporating varying borehole diameter. Iteration has continued until the short-, intermediate-, and long-spacing electrical logs match with those derived from forward modelling the layered model. Residual differences on the ultra-long spacings have then been interpreted in terms of conductive fractured zones remote from the wellbore by tens of metres. This interpretation has been done by further application of the 2D finite element code with a remote axisymmetric conductive zone. This has finally been interpreted in terms of distance to the remote fractured zone in a 3D geometry by means of a 3D Laplace's Equation finite element code.

28/3,AB/31 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05245684 JICST ACCESSION NUMBER: 02A0706215 FILE SEGMENT: JICST-E
S-Band 38dBm Power Amplifier Using PHEMT and **FR4** Substrate.
LIU H Z (1); WANG Y H (1); HSU C C (2); CHANG C H (2); WU W (2); WU C L (2); CHANG C S (2)
(1) National Cheng-kung Univ., Tainan, Twn; (2) Transcom, Inc., Tainan, Twn
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 2002, VOL.102,NO.179(SDM2002 107-121), PAGE.29-32, FIG.9, REF.12
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.375
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A high performance S-band power amplifier fabricated on a low cost 20-mil thick **FR4** substrate is demonstrated. The amplifier consists of a single-ended driver amplifier and a balanced output power amplifier by utilizing Wilkinson power dividers/combiners with quarter-wave transmission lines. The S-band power amplifier with 38dBm output power, 25.6% power-added efficiency(PAE), 3.9dB noise figure and 22dB small-signal gain is reported. In addition, excellent linearity with 48.25dBm third-order intercept point is achieved. (author abst.)

28/3,AB/32 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04911353 JICST ACCESSION NUMBER: 01A0632303 FILE SEGMENT: JICST-E
Flashover Characteristics between Foil Conductors on a Printed Wiring Board.
TAKAOKA YOSUKE (1); YAMANO YOSHIAKI (1)
(1) Chiba Univ.
Denki Gakkai Yuden, Zetsuen Zairyo Kenkyukai Shiryo, 2001, VOL.DEI-01,NO.81-87, PAGE.21-26, FIG.8, REF.3
JOURNAL NUMBER: Z0908BAX
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.75 621.315.6
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Surface flashover voltage between wiring conductors on a printed wiring board was studied in air at a room temperature and a relative humidity less than 40%. The material of the printed wiring board is glass-epoxy FRP (**FR4**). An impulse voltage (0.5/6.MU.s) was applied between the conductors. The distance between the conductors ranges from 30.MU.m to 500.MU.m. The experimental results suggest that the impulse flashover voltages(FOVs) along the surface between the conductors in the distance range are higher than those for the homogeneous field in the case of the board without earthed backside electrode. In the case of the board with the backside electrode, the FOV on the board at the distance of 500.MU.m is slightly lower than that of the air space. However, in the distance area shorter than 400.MU.m, the FOVs on the board are higher than those in the homogeneous field. (author abst.)

28/3,AB/33 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03787122 JICST ACCESSION NUMBER: 98A0934562 FILE SEGMENT: JICST-E
TOKIN the 60th Anniversary. Progress and Perspective & Technologies in Business Units. **Multi-Layered** Chip Components.
SATO HIROYUKI (1)
(1) Tokin Corp.
Tokin Tech Rev, 1998, VOL.25, PAGE.26-30, FIG.7
JOURNAL NUMBER: Y0462ABR ISSN NO: 0916-0728
UNIVERSAL DECIMAL CLASSIFICATION: 621.316.8+621.318.3/.4
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Introduction article
MEDIA TYPE: Printed Publication
ABSTRACT: The super-miniaturization of **passive components** fabricated by using **multi-layered** technology is indispensable to the development of multi-functional and compact **electronic devices** for mobile equipment. Our company has been engaged into developing the chip capacitors and inductors by developing the **multi-layered** technology and the relative material technologies. In this paper, taking the **multi-layered** inductor as an example, the production process of the components using the previous **multi-layered** technology and function improvement is described. As the technologies in thin film, semiconductor and so on are combined into the **multi-layered** technology, these components will be eventually more compact, more functional and more integrated. (author abst.)

28/3,AB/34 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03536239 JICST ACCESSION NUMBER: 98A0029690 FILE SEGMENT: JICST-E
Present state and new challenge of surface **mounting** technology.
HONDA TATSUO (1)
(1) Honda Jimusho
Denshi Gijutsu(Electronic Engineering), 1997, VOL.39,NO.12, PAGE.96-100, FIG.8, REF.20
JOURNAL NUMBER: F0571AAK ISSN NO: 0366-8819 CODEN: DEGIA
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.75
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes a problem from a surface **mounting** technology to a further new technology. In soldering of **passive components** and assembling of semiconductor devices, combination of circuit components and chip size package CSP are mentioned. On substrates, buildup substrates and other substrates are mentioned. On the latest packaging technology, 20 literatures are mentioned.

28/3,AB/35 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02384361 JICST ACCESSION NUMBER: 95A0472299 FILE SEGMENT: JICST-E
Method of taking in surface **mount passive components** into a package.
WATANABE HIROSHI (1)
(1) Toshiba Corp.

Toshiba Gijutsu Kokaishu, 1995, VOL.13,NO.29, PAGE.21-22, FIG.2
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

28/3,AB/36 (Item 6 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02312657 JICST ACCESSION NUMBER: 95A0193378 FILE SEGMENT: JICST-E
Electronic device for mobil radio communication equipment.
Latest trends of surface **mounting** parts for mobil radio communications.
NAKAI SHIN'YA (1)
(1) TDK Corp.
Denshi Zairyo(Electronic Parts and Materials), 1995, VOL.34,NO.2, PAGE.22-26, FIG.10, REF.1
JOURNAL NUMBER: F0040AAH ISSN NO: 0387-0774
UNIVERSAL DECIMAL CLASSIFICATION: 621.396.73 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: General **passive components**, active components such as LSI and IC and compound functional parts, are separately described to introduce, present state and trends of surface **mounting** parts including automatic attachment method. Chip capacitors, chip resistances, and chip inductors are increasingly being miniaturized to 1.0*0.5mm in size or smaller. To LSI's, 0.5mm-pitch QFP makes a large contribution. Duplexers, isolators, and filters are also commercialized.

28/3,AB/37 (Item 7 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02032104 JICST ACCESSION NUMBER: 94A0438312 FILE SEGMENT: JICST-E
Reliability of **Electronic Devices** at High Temperature.
KOJIMA TAKESHI (1); TAKAHISA KIYOSHI (1); KUMAGAI MASAO (1); ISHIZAKI YASUO (1)
(1) Electrotech. Lab., Agency of Ind. Sci. and Technol.
Denshi Gijutsu Sogo Kenkyujo Iho(Bulletin of the Electrotechnical Laboratory), 1994, VOL.58,NO.3, PAGE.201-208, FIG.16, TBL.1, REF.8
JOURNAL NUMBER: F0014ABN ISSN NO: 0366-9092
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The upper operating temperature for conventional **electronic devices** mainly composed of Si devices and organic materials is limied to 200.DEG.C.. On the other haud, SiC devices and diamond devices have recently been developed to function at up to 500.DEG.C. and are expected to be applied for high temperature. The problem to operate **electronic circuits** stably for long period at high temperatures is thermal degradation and interdiffusion between

materials. In this paper, **conductive**, **resistive** and insulating materials which can be operated under 300.DEG.C. are investigated. Also the experimental results of metal diffusion into SiC crystal is reported. (author abst.)

28/3,AB/38 (Item 8 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01811667 JICST ACCESSION NUMBER: 93A0756595 FILE SEGMENT: JICST-E
Degradation of **electronic devices** in high temperature.
KOJIMA TAKESHI (1); TAKAHISA KIYOSHI (1); YANAGISAWA TAKESHI (1); KUMAGAI MASAO (2); KONDO TOSHIYUKI (2)
(1) Electrotechnical Lab.; (2) Kanagawakodogijutsushienzaidan
Nippon Kikai Gakkai Kikai Rikigaku, Keisoku Seigyo Koen Ronbunshu, 1993, VOL.1993,NO.B, PAGE.299-303, FIG.13, REF.5
JOURNAL NUMBER: L1497AAE
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: 200.DEG.C. is the temperature limit for conventional **electronic device** chiefly Si device and organic material to function stably. SiC device and diamond device have been recerty developed to function at up to 500.DEG.C. and are expected to beapplied for high temperature. The problem to operate **electronic circuits** stably for long period at high temperature is thermal degradation and diffusion between materials. In the paper, **conductive**, **resistive** and insulated materials which can operate under 300.DEG.C. are investigated. Also the experimental result of metals diffusion into SiC crystal is reported. (author abst.)

28/3,AB/39 (Item 9 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00408606 JICST ACCESSION NUMBER: 87A0224858 FILE SEGMENT: JICST-E
Passive components and hybrid technology.
NOMURA TAKESHI (1); TAKAYA MINORU (1)
(1) TDK Kaiken
Hybrids, 1987, VOL.3,NO.1, PAGE.16-19,15, FIG.6
JOURNAL NUMBER: S0579BAC ISSN NO: 0914-2568
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.049.77 621.316.8+621.318.3/.4
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

28/3,AB/40 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

2275180 H.W. WILSON RECORD NUMBER: BAST01029427
An integrated micro cooling system for **electronic circuits**
Schutze, Jorg; Ilgen, Herman; Fahrner, Wolfgang R
IEEE Transactions on Industrial Electronics v. 48 no2.(Apr. 2001) p. 281-5
DOCUMENT TYPE: Feature Article ISSN: 0278-0046

ABSTRACT: The authors developed a fully **FR4**-compatible integrated cooling system. Cooling channels were etched into a thick copper layer to form microchannels. The structure was strengthened by 2 prepeg layers toward the component and solder side. A number of cooling channels can be run independently. The heat dissipation capability of the system is 20 W per channel, and pressure losses are less than 300 mbar.

28/3,AB/41 (Item 2 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1597955 H.W. WILSON RECORD NUMBER: BAST96000824
Aluminum nitride high power terminations
Microwave Journal v. 38 (Dec. '95) p. 114+
DOCUMENT TYPE: Feature Article ISSN: 0192-6225

ABSTRACT: AlN has recently found use as a substitute for BeO in high-power devices and applications. New procedures have recently been developed that allow **resistive** and **conductive** films to adhere reliably to the AlN material. Consequently, a line of high-power flange terminations has been developed and is now available on the market.

28/3,AB/42 (Item 3 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1241363 H.W. WILSON RECORD NUMBER: BAST95037097
Manufacturing dielectric powders
Chu, Mike S. H; Rae, Alan W. I. M
American Ceramic Society Bulletin v. 74 (June '95) p. 69-72
DOCUMENT TYPE: Feature Article ISSN: 0002-7812

ABSTRACT: The use of dielectric ceramic material in the manufacture of **multilayer** ceramic capacitors (MLCCs) is reviewed. The MLCC has been the main **passive component** in **electronic circuitry** in the past 20 years, with an estimated 125 billion produced in 1994 alone. The selection of the proper powder to use in the manufacturing process is an important strategic decision for a ceramic component manufacturer, who must consider certain critical parameters, such as performance, processing conditions, and cost of ownership of the powder.

28/3,AB/43 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

09643904 PASCAL No.: 91-0441028
Surface film technique for crack length measurement in nonconductive brittle materials : calibration and evaluation
OGAWA T; SURESH S
Brown univ., div. eng., Providence RI 02912, USA
Journal: Engineering fracture mechanics, 1991, 39 (4) 629-640 (11 p.)
Language: English
A carbon film deposit technique is described. The carbon layer is connected to an **electrical circuit** which have an electrical resistance depending on the crack length. The high precision and reliability are demonstrated with the aid of experimental results with Y-TZP, Mg-PSZ ceramic and a polycrystalline Al SUB 2 O SUB 3 .